PCI Express M.2 Specification

Revision 1.1

December 9, 2016

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Revision History

Rev	Version	History	Date
1.0		**Initial Release**	November 1, 2013
1.1		**Incorporated the following ECNs:** • Transition of NFC Signals from 3.3 V to 1.8 V ECN • M.2 COEX Signal Definition – UART ECN • M.2 2242 WWAN Module ECN • M.2 Signal Definition – Audio ~~&~~and ANTCTL Functions ECN • Tx Blanking and SYSCLK on Socket 1 Related Pinouts ECN • Power-up Requirements for PCIe Side Bands (PERST#, etc.) ECN • Power-up Requirements for PCIe Side Bands in a V_{BAT} Powered System ECN • MiniEx_M2_ECN_SMBus_for_SSD_Socket2_Socket3 - 1112_14 • WWAN_Key_C_Definition_ECN_WW12.3 • SMBus ECN, Clarification • BGA-SSD ECN • M.2 SSIC Eye Limits Definitions **Other changes:** • Incorporated all changes from *M2_10 Errata Table and Backup of M 2 Rev1 0 Errata Table 04292015-6.8.* • Added section 6.8, *High Speed Differential Pair AC Coupling Cap Values and Cap Location Examples* • Changed all Mid-Line and Mid-plane to Mid-mount per WG decision • Clarified the terms Module, Add-in Card, Adapter • Capitalized Platform • Removed all + signs from voltages • Updated per *PCI SIG Style Guide* • Updated specification to USB3.1 Gen1 • Added *MIPI Alliance Specification for RF Front-End Control Interface (RFFE*[SM]*),* Version 2.0, September 25, 2014 to section 1.3	December 9, 2016

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1

1. Introduction to M.2 Specification

The M.2 form factor is intended for Mobile ~~Add-In cards~~Adapters. The M.2 is a natural transition from the Mini Card and Half-Mini Card (refer to the *PCI Express Mini CEM Specification*) to a smaller form factor in both size and volume. The M.2 is a family of form factors that ~~will~~ enables expansion, contraction, and higher integration of functions onto a single form factor module solution.

The key target for M.2 is to be significantly smaller in the XYZ and overall volume of the Half-Mini Card used today in mobile ~~Platform~~Platforms in preparation for the very thin computing ~~Platform~~Platforms (~~for example~~e.g., Notebook, Tablet/Slate ~~Platform~~Platforms) that require a much smaller solution.

The M.2 comes in two main formats:

- Connectorized
- Soldered-down

Figure 1 shows the concept board Add-in Card and M~~m~~odule~~s~~.

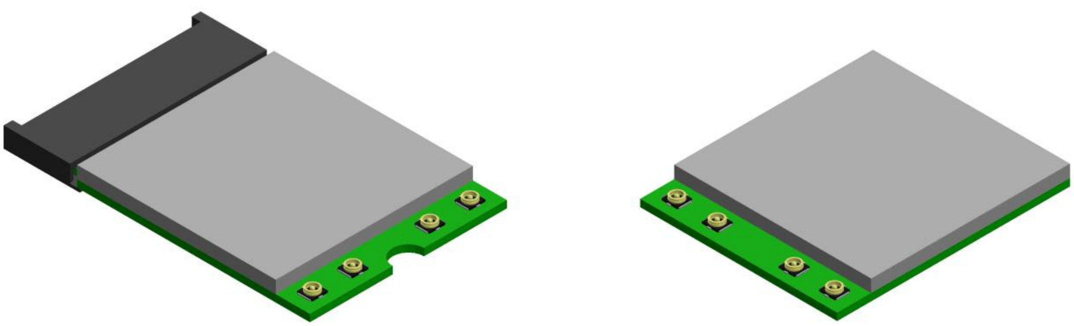


Figure 1. M.2 Concept ~~Board/~~Add-in Card and Module~~s~~

M.2 is targeted toward addressing system manufacturers' needs for build-to-order (BTO) and configure-to-order (CTO) rather than providing a general end-user-replaceable ~~module~~Adapter. ~~As such, the requirements provided in this document should be viewed in their entirety as an optional normative specification.~~ It is expected that system manufacturers that build to and order modules to this specification are responsible for indicating to their module suppliers which aspects of the specification are normative, optional, or explicitly not required for the products being ordered.

1.1. Terms and Definitions

Adapter	Used generically to refer to an Add-in Card or Module.
Add-in Card	A card that is plugged into a connector and mounted in a chassis socket.
Host	Typically referring to the electrical interface source/master.
Module	Device that is soldered down to the Platform motherboard.
~~Platform~~Platform	Typically referring to the system within which a Main Board or Mother Board (MB) is located, to which the Module or Add-in Card are mounted.~~Typically referring to the physical location. Usually a Mother Board on which the Module/Add-in Card are mounted (connectorized or soldered down)~~
~~Module~~	~~The Add-in card or device that is either plugged into the Platform connector or soldered down onto the Platform Mother Board~~
~~Add-in Card~~	~~A card or module that is plugged into a connector and mounted in a chassis socket.~~
x1, x2, x4	x1 refers to one Lane of basic bandwidth. x2 refers to a collection of two Lanes. ~~;~~x4 refers to a collection of four Lanes~~; etc~~. This is applicable to PCIe, Display Port and other host interfaces that are permitted to use multi-Lane~~to PCIe and Display Port signals that may use Multi-lanes~~.

1.2. Targeted Application

~~The~~ This M.2 family of form factors is intended to support multiple function ~~add-in cards/modules~~Adapter that include the following:

- Wi-Fi
- Bluetooth
- Global Navigation Satellite Systems (GNSS)
- Near Field Communication (NFC)
- WiGig
- WWAN (2G, 3G, and 4G)
- Solid-State Storage Devices (SSD)

- Other ~~&~~ and Future Solutions (e.g., Hybrid Digital Radio (HDR))

~~The M.2 Specification will~~This specification covers multiple Host Interface solutions including:

- PCIe, PCIe LP
- HSIC
- SSIC
- M-PCIe
- USB
- SDIO
- UART
- PCM/I2S
- I^{2}C
- SMBus
- SATA
- Display Port
- All future variants of the interfaces in this list

In light of the fact that the number of host interfaces has dramatically increased and in order to support the multitude of Comms and other solutions typically integrated into ~~NB~~Notebook (NB)-based and very thin-based ~~Platform~~Platforms, there is a need to clearly define several distinct sockets:

- Connectivity Socket (typically Wi-Fi, BT, NFC or Wi-Gig) designated as Socket 1
- WWAN/SSD/Other Socket that will support various WWAN+GNSS solutions, various SSD and SSD Cache configurations and potentially other yet undefined solutions designated as Socket 2
- SSD Drive Socket with SATA or up to 4 lanes of PCIe designated as Socket 3

Each of the three sockets is unique and incorporates a different collection of host interfaces to support the specific functionality of the ~~modules~~Add-in Card. The Add-in Cards ~~modules~~ are typically not interchangeable between sockets. Therefore, each Socket will have a unique mechanical key. However, there are cases where a dual mechanical key scheme will enable dual socket support. Details of the sockets will be described in the following sections of this document.

! CAUTION: M.2 Add-in Card are not designed or intended to support Hot-Swap or Hot-Plug connections. Performing Hot-Swap or Hot-Plug may pose danger to the M.2 Add-in Card~~module~~, to the system ~~Platform~~Platform, and to the person performing this act.

For the sake of coverage, the ~~connectorized~~ M.2 Add-in Card ~~boards/modules~~ will be defined as both single-sided for low profile solutions and double-sided to enable more content to be integrated in the ~~Platform~~Platform. Several target Z-heights will be outlined as part of the specification. Actual configuration implementation will be determined between customer and vendor. A naming convention will enable an exact definition of all key parameters.

1.3. Specification References

This specification requires references to other specifications or documents that will form the basis for some of the requirements stated herein.

- *PCI Express Mini Card Electromechanical (CEM) Specification*, Revision 2.0
- *PCI Express Card Electromechanical (CEM) Specification*, Revision 3.0
- *Advanced Configuration and Power Interface (ACPI) Specification*, Revision 2.0b
- *PCI Express Base Specification*, Revision 3.1
- SDIO3.0
- SSIC – *SuperSpeed USB Inter-Chip Supplement to the USB 3.0 Specification*, Revision 1.0 as of May 3, 2012
- HSIC - *High-Speed Inter-Chip USB Electrical Specification*, Version 1.0 (September 23, 2007), plus *HSIC ECN Disconnect Supplement to High Speed Inter Chip Specification*, Revision 0.94 (Sep 20, 2012)
- USB2.0 - *Universal Serial Bus Specification*, Revision 2.0, plus ECN and Errata, July 14, 2011, available from http://www.usb.org
- USB3.1 - *Universal Serial Bus Specification*, Revision 3.1, plus ECN and Errata, available from http://www.usb.org
- *DisplayPort Standard Specifications*, version 1.2
- *ISO/IEC 7816-2 Specification*
- *ISO/IEC 7816-3 Specification*
- *Serial ATA Specification*, available from www.sata-io.org
- *I^{2}C BUS Specifications*, Version 2.1, January 2000
- *EIA-364 Electrical Connector/Socket Test Procedures* including Environmental Classifications
- *EIA*-364-1000.01: *Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications*
- *M-PHY - MIPI Alliance Specification* for M-PHY, Version 3.0
- *MIPI Alliance Specification for RF Front-End Control Interface (RFFE^{SM}),* Version 2.0, September 25, 2014
- *JTAG Specification* (IEEE 1149.1), available from https://www.ieee.org
- *System Management Bus (SMBus) Specification*, Version 2.0, August 3, 2000, available from http://smbus.org/
- *BT-SIG – Draft Improvement Proposal Document* for Coexistence, v10r00, January 19, 2010

2

2. Mechanical Specification

2.1. Overview

This specification defines a family of M.2 ~~modules~~ Adapters and the corresponding system interconnects based on a 75 position edge card connection scheme or a derivation of the card edge and a soldered-down scheme for system interfaces.

The M.2 family comprised of several ~~module~~ Adapter sizes and designated by the following names (see Figure 2):

- Type 1216
- Type 1620
- Type 1630
- Type 2024
- Type 2226
- Type 2228
- Type 2230
- Type 2242
- Type 2260
- Type 2280
- Type 2828
- Type 3026
- Type 3030
- Type 3042
- Type 22110

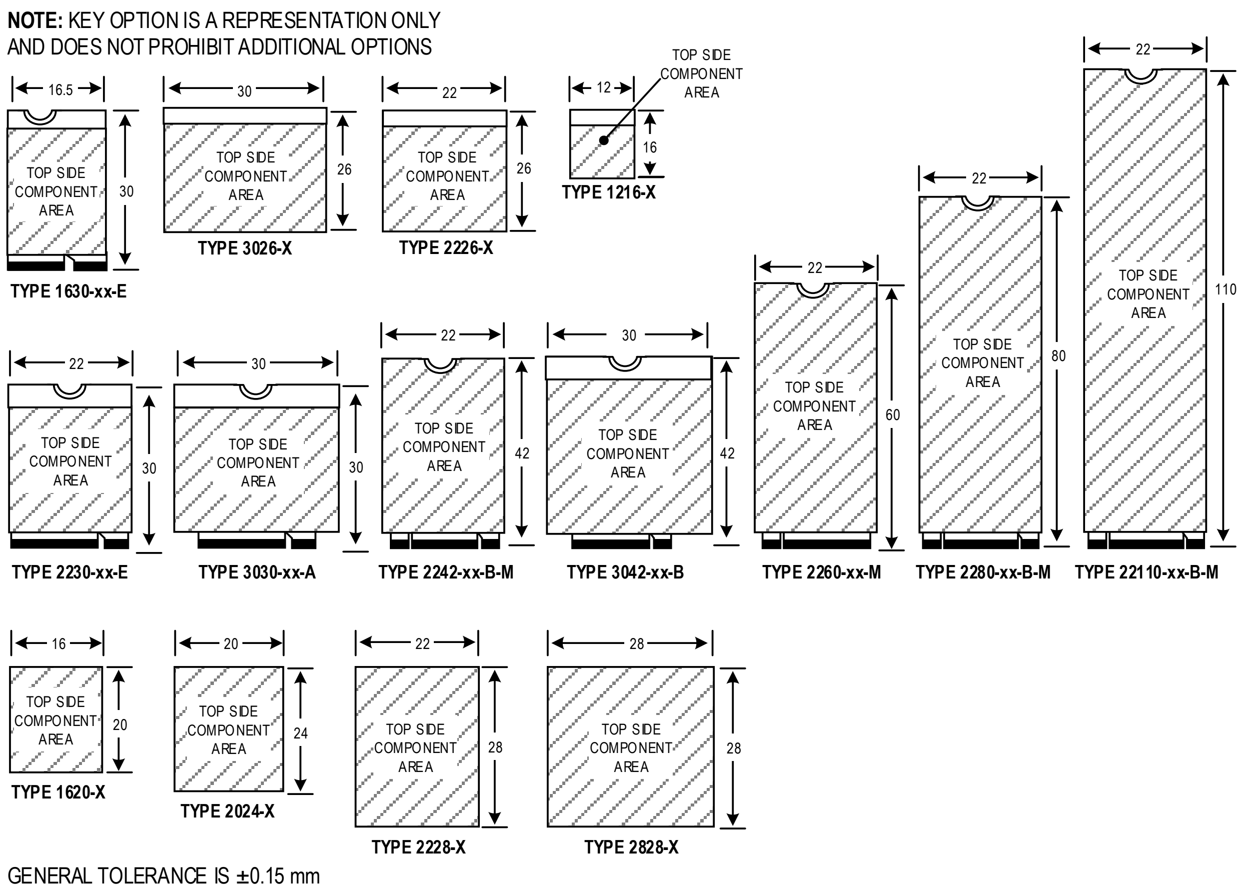


Figure 2. M.2 Family of Form Factors

The majority of M.2 types are connectorized using an edge connection scheme that ~~can be~~is either~~ a~~ single-sided or double-sided assembly. There will be several component Z-height options defined in this specification. The type of edge connector will cater to different P~~p~~latform Z-height requirements. In all cases, the board thickness is 0.8 mm ±10%. The Type 1216, Type 2226, and Type 3026 are soldered down solutions that have a~~n~~ Land Grid Array (LGA) pattern on the back. Therefore, they ~~can only be~~are single-sided and the board thickness does not need to adhere to the 0.8 mm ±10% requirement. The Type 1620, Type 2024, Type 2228, and Type 2828 are soldered-down solutions that have Ball Grid Array (BGA) pattern on the back and are defined for BGA SSDs. These BGA solutions ~~can be~~are placed directly on host ~~platforms~~ Platforms as standalone BGA SSDs (see S~~s~~ection 3.4 ~~3.4~~ for the interface specification). Some BGA types ~~can also be~~are mounted on SSD Socket 2 or SSD Socket 3 Add-in Cards ~~modules~~ (see ~~sections~~ Sections 3.2 ~~3.2~~ and 3.3 ~~3.3~~ for interface specification). When a BGA SSD is mounted on SSD Socket 2 or SSD Socket 3 Add-in Cards~~modules~~, the Add-in Card ~~module~~ is responsible for implementing the voltage conversion circuitry to provide 1.8 V and 1.2 V as required.

The edge connector requires a mechanical key for accurate alignment. The location of the mechanical key along the Gold Finger contacts will make each key unique per a given socket connector. This prevents wrongful insertion of an incompatible board which prevents a safety hazard.

The board type, the type of assembly, the component Z-heights on top and bottom, and the mechanical key will make up the M.2 board naming convention detailed in the next section.

2.2. Card Type Naming Convention

Since there are various types of M.2 solutions and configurations, a standard naming convention will be employed to define the main features of a specific solution.

The naming convention will identify the following:

- The ~~module~~ Adapter size (width ~~&~~ and length).
- The component assembly maximum Z-height for the top and bottom sides of the ~~module~~Adapter.
- The Mechanical Connector Key/~~Module~~ Add-in Card key location/assignment or multiple locations/assignments

These naming conventions will clearly define the ~~module~~ Adapter functionality, what connector it coincides with, and what Z-heights are met. Figure 3 diagrams the naming convention.

The ~~module~~ Adapter width options are~~:~~ 12 mm, 16 mm, 16.5 mm, 20 mm, 22 mm, 28 mm, and 30 mm.

The ~~module~~ Adapter length ~~can~~ scales to various lengths to support the content and expand as the content increases. The lengths supported are 16 mm, 20 mm, 24 mm, 26 mm, 28 mm, 30 mm, 42 mm, 60 mm, 80 mm, and 110 mm.

Together these two dimensions make up the first part of the ~~module~~ Adapter type definition portion of the Adapter name.

The next part of the name describes whether the ~~module~~ Adapter is single-sided or double-sided and a secondary definition of what are the maximum Z-heights of the components on the top and bottom side of the ~~module~~Adapter. Here we have specific Z-height limits that are either 2.0 mm, 1.75 mm, 1.5 mm, 1.35 mm, or 1.2 mm on the top-side and 1.5 mm, 1.35 mm, 0.7 mm and 0 mm on the bottom side. The letter S will designate Single-sided and the letter D will designate Double-sided. This will be complimented with a number that designates the specific Z-height combination option.

The last section of the name will designate the mechanical connector key/~~module~~ Add-in Card key name and the coinciding pin location. These will be designated by a letter from A to M. In cases where the Add-in Card ~~module~~ will have a dual key scheme to enable insertion of the Add-in Card ~~module~~ into two different keyed sockets, a second letter will be added to designate the second mechanical connector key/Add-in Card ~~module~~ key.

Key ID assignment must be approved by the PCI-SIG. Unauthorized Key IDs would render the Add-in Card ~~modules~~ incompatible with ~~the M.2~~this specification.

Figure 4 ~~on the following page~~ shows an example of Add-in Card ~~module~~ Type 2242 – D2 – B – M.

Adapter Nomenclature
Sample Type 2242-D2-B-M

Type XX XX – XX – X - X*

Width (mm)
12
16
20
22
28
30

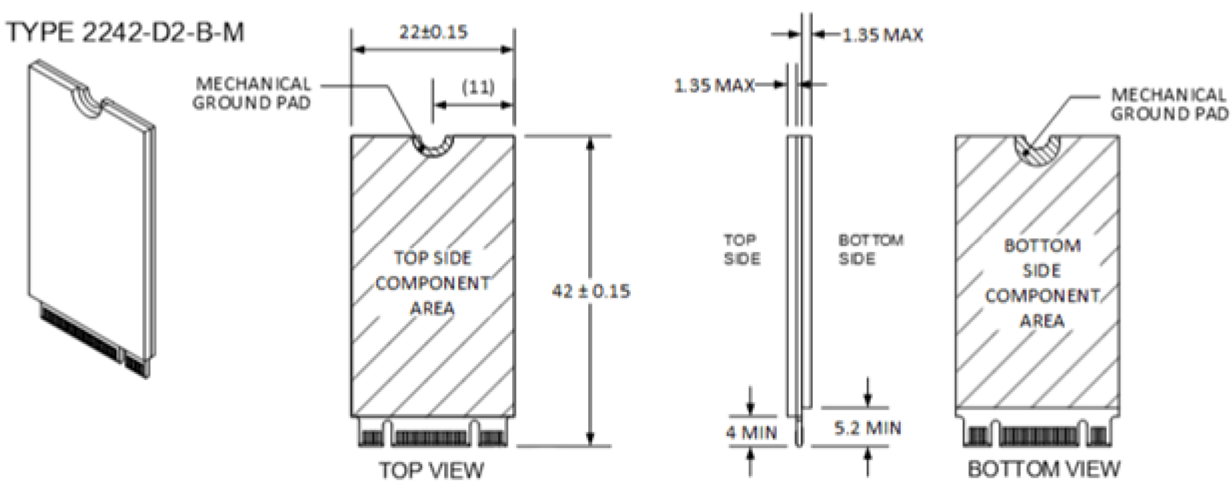
Length (mm)
16
20
24
26
28
30
42
60
80
110

Label**	Component Max Ht (mm)	
	Top Max	Bottom Max
S1	1.2(1)	0****
S2	1.35(1)	0****
S3	1.5(1)	0****
S4	1.75(1)	0****
S5	2.0(1)	0****
D1	1.2	1.35
D2	1.35	1.35
D3	1.5	1.35
D4	1.5	0.7
D5	1.5	1.5

Key ID	Pin	Interface
A	8-15	2x PCIe x1/USB 2.0/I2C/DP x4
B	12-19	PCIe x2/SATA/USB 2.0/USB 3.1 Gen1/HSIC/SSIC/Audio/UIM/I2C/SMBus
C	16-23	PCIe/M-PCIe/USB 2.0/USB 3.1 Gen1/SSIC/I2C-SlimBus/UIM/ANTCTL
D	20-27	Reserved for Future Use (RFU)
E	24-31	2x PCIe x1/USB 2.0/I2C/SDIO/UART/PCM
F	28-35	Future Memory Interface (FMI)
G	39-46	Generic (Not used for M.2)***
H	43-50	RFU
J	47-54	RFU
K	51-58	RFU
L	55-62	RFU
M	59-66	PCIe x4/SATA/SMBus

* Use ONLY when a double slot is being specified.
** Label included in height dimension.
*** Key G is intended for customer use. Devices with this key will not be M.2 compliant. Use at your own risk.
**** Insulating label allowed on connector-based design.
(1) For BGA SSD, Max Height is measured with solder balls collapsed and is valid whether BGA is located directly on a Platform or mounted on an Add-in Card.

Figure 3. M.2 Naming Nomenclature



Note: For card-edge details, see ~~s~~Section 2.3.4.~~, Card PCB Details~~

Figure 4. Example of Type 2242-D2-B-M Nomenclature

The board is 22 mm x 42 mm, Double-sided with a maximum Z-height of 1.35 mm on both the Top and Bottom, and it has two mechanical connector keys/ Add-in Card ~~module~~ keys at locations B and M which will enable it to plug into two types of connectors (Key B or Key M).

~~Table 1~~See Table 1 ~~shows~~ for the various options for board configurations as a function of the Socket, ~~Module~~ Adapter Function, and ~~Module~~ Adapter size.

Type 1216, Type 1620, Type 2024, Type 2226, Type 2228, Type 2828, and Type 3026 are unique as they are Soldered-Down solutions while all the others are connectorized with a PCB Gold Finger layout that coincides with an Edge Card connector. The Soldered-Down solutions do not have mechanical keys and their pinout configuration needs to be specifically called out.

Table 1. Optional ~~Module~~ Adapter Configurations

	Soldered-down			Connectorized			
	Type	Module Height Options	Pinouts Key	Connector Key	Type	Add-in Card ~~Module~~ Height Options	Module Key
Socket 1 Connectivity	1216	S1, S3	E	N/A	N/A	N/A	N/A
	N/A	N/A	N/A	A, E	1630	S1, D1, S3, D3, D4	A, E, A+E
	2226	S1, S3	E	A, E	2230	S1, D1, S3, D3, D4	A, E, A+E
	3026	S1, S3	A+E	A, E	3030	S1, D1, S3, D3, D4	A, E, A+E
Socket 2 WWAN/ Other	N/A	N/A	N/A	B, C	3042	S1, D1, S3, D3, D4	B, C
	N/A	N/A	N/A	B, C	2242	S1, D1, S3, D3, D4	B, C
Socket 2 SSD/Other	N/A	N/A	N/A	B	2230	S2, D2, S3, D3, D5, S4, S5	B+M
	N/A	N/A	N/A	B	2242	S2, D2, S3, D3, D5, S4, S5	B+M
	N/A	N/A	N/A	B	2260	S2, D2, S3, D3, D5, S4, S5	B+M
	N/A	N/A	N/A	B	2280	S2, D2, S3, D3, D5, S4, S5	B+M
	N/A	N/A	N/A	B	22110	S2, D2, S3, D3, D5, S4, S5	B+M
	1620	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	2024	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	2228	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	2828	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
Socket 3 SSD Drive	N/A	N/A	N/A	M	2230	S2, D2, S3, D3, D5, S4, S5	M, B+M
	N/A	N/A	N/A	M	2242	S2, D2, S3, D3, D5, S4, S5	M, B+M
	N/A	N/A	N/A	M	2260	S2, D2, S3, D3, D5, S4, S5	M, B+M
	N/A	N/A	N/A	M	2280	S2, D2, S3, D3, D5, S4, S5	M, B+M
	N/A	N/A	N/A	M	22110	S2, D2, S3, D3, D5, S4, S5	M, B+M
	1620	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	2024	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	2228	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A
	2828	S1, S2, S3, S4, S5	N/A	N/A	N/A	N/A	N/A

2.3. Card Specifications

There are multiple defined card outlines. Card thickness is fixed at 0.8 mm ±10% with optional increased/decreased XY dimensions so as to incorporate more or less functionality on the board.

For purposes of the drawings in this specification, the following notes apply:

- All dimensions are in millimeters (mm), unless otherwise specified.
- All dimension tolerances are ± 0.15 mm, unless otherwise specified.
- Insulating material ~~shall~~ must not interfere with or obstruct mounting holes or grounding pads.
- The Add-in Card ~~board/module~~ has a 4 mm tall strip at the lower end of the board intended to support the Gold Finger pads used in conjunction with an Edge Card connector. The Gold Fingers appear on both top and bottom side of the Add-in Card PCB.
- In some configuration, the Adapter ~~board/module~~ has a 3.8 mm strip intended to support Radio Frequency (RF) connectors.
- All connectorized versions have a mounting/retention screw (half-moon cutout) at the upper end of the Add-in Card ~~board/module~~ used to hold down the Add-in Card ~~board~~ onto the m~~M~~otherboard or chassis.
- The remainder of the board area available is intended for Active Components but not limited to this. Encroachment into this area ~~can be done~~is permitted if extra area is needed for additional RF antenna connectors.
- The diagrams showing mechanical connector key/Add-in Card ~~module~~ key locations in this document are for example only. Actual Key location/definition is part of the actual ~~module~~ Adapter name per the naming convention.
- General Tolerance Summary as given in Table 2.

Table 2. General Tolerance

	+ Plus	– Minus
PCB Size Tolerance	0.15 mm	0.15 mm
PCB Thickness	0.08 mm	0.08 mm
Bevel Capabilities	0.25 mm	0.25 mm
Drill Capabilities for Add-in Card ~~Module~~ key	0.05 mm	0.05 mm

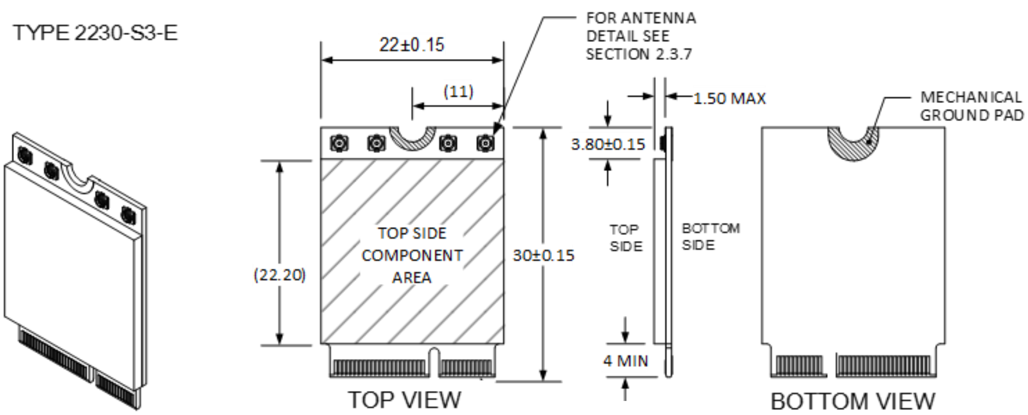
2.3.1. Card Form Factors Intended for Connectivity Socket 1

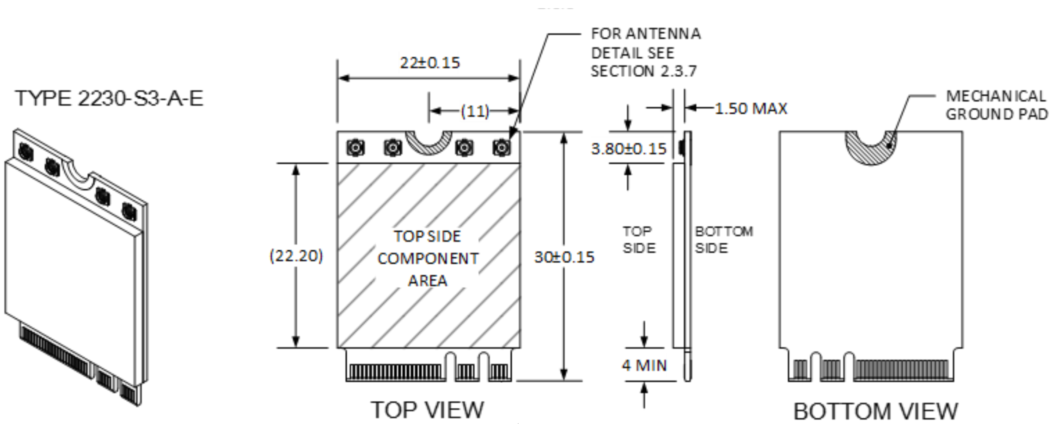
2.3.1.1. Type 2230 Specification

The Generic ~~M.2 board/module~~Adapter size used for the majority of the Connectivity solutions such as Wi-Fi+BT type solutions is Type 2230. ~~However, t~~This board size ~~can also~~also is permitted to accommodate other Multi-Comm and Combo solutions~~ as well~~.

The Type 2230 Add-in Card ~~board/module~~ is intended to support the multiple Wi-Fi configurations such as 1x1, 2x2, and 3x3. An example of the Type 2230 Add-in Card ~~board/module~~ mechanical outline drawing is shown in Figure 5 and Figure 6.

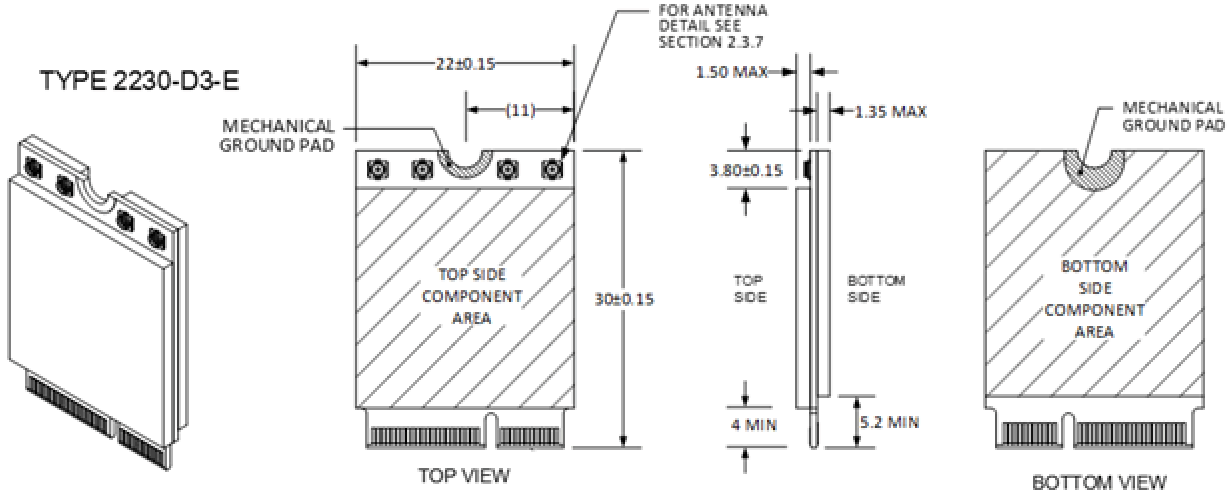
The Type 2230 Add-in Card ~~board/module~~ uses a 75 position host interface connector and has room to support up to four ~~(4)~~ RF connectors in the upper section. The recommended location and assignment of the four RF connectors is described in ~~s~~Section 2.3.7~~, *RF Connectors*~~. RF connectors ~~may~~ are permitted to be placed in other locations on the Type 2230 Add-in Card~~board/module~~. In cases where additional RF connectors are needed, they are permitted to ~~can~~ be added in the active component area and should maintain a minimal distance of 4.5 mm center-to-center to enable manufacturing test interface of the RF connection.

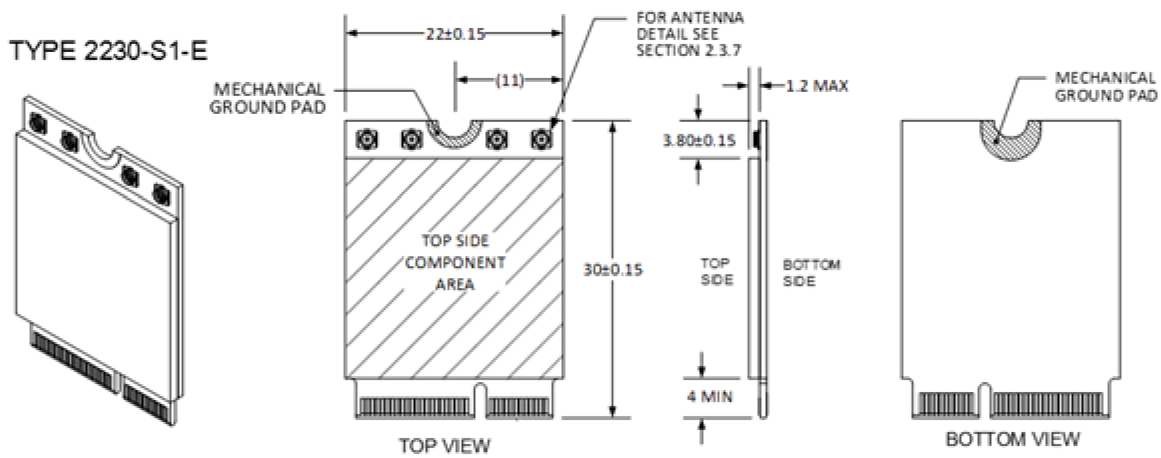




Note: For card-edge details, see Ssection 2.3.4.~~, Card PCB Details~~

Figure 5. M.2 Type 2230-S3 Mechanical Outline Drawing Examples





Note: For card-edge details, see S~~s~~ection 2.3.4.~~, Card PCB Details~~

Figure 6. M.2 Type 2230-D3/S1 Mechanical Outline Drawing Examples

2.3.1.2. Type 1630 Specification

Type 1630 is a smaller M.2 Add-in Card ~~board/module~~ size used for single Comm or more simplistic Comm combo solutions such as Wi-Fi 1x1 or 2x2 + BT only or future multi-comm solutions that ~~can~~ fits in a smaller footprint.

The Type 1630 is a subset of the Type 2230 board with 5.5 mm sliced off along the entire length of the board. Therefore, it is inherently limited in the number of RF connections and has a reduced number of pins used in the Host Interface connector. Because the Type 1630 Add-in Card

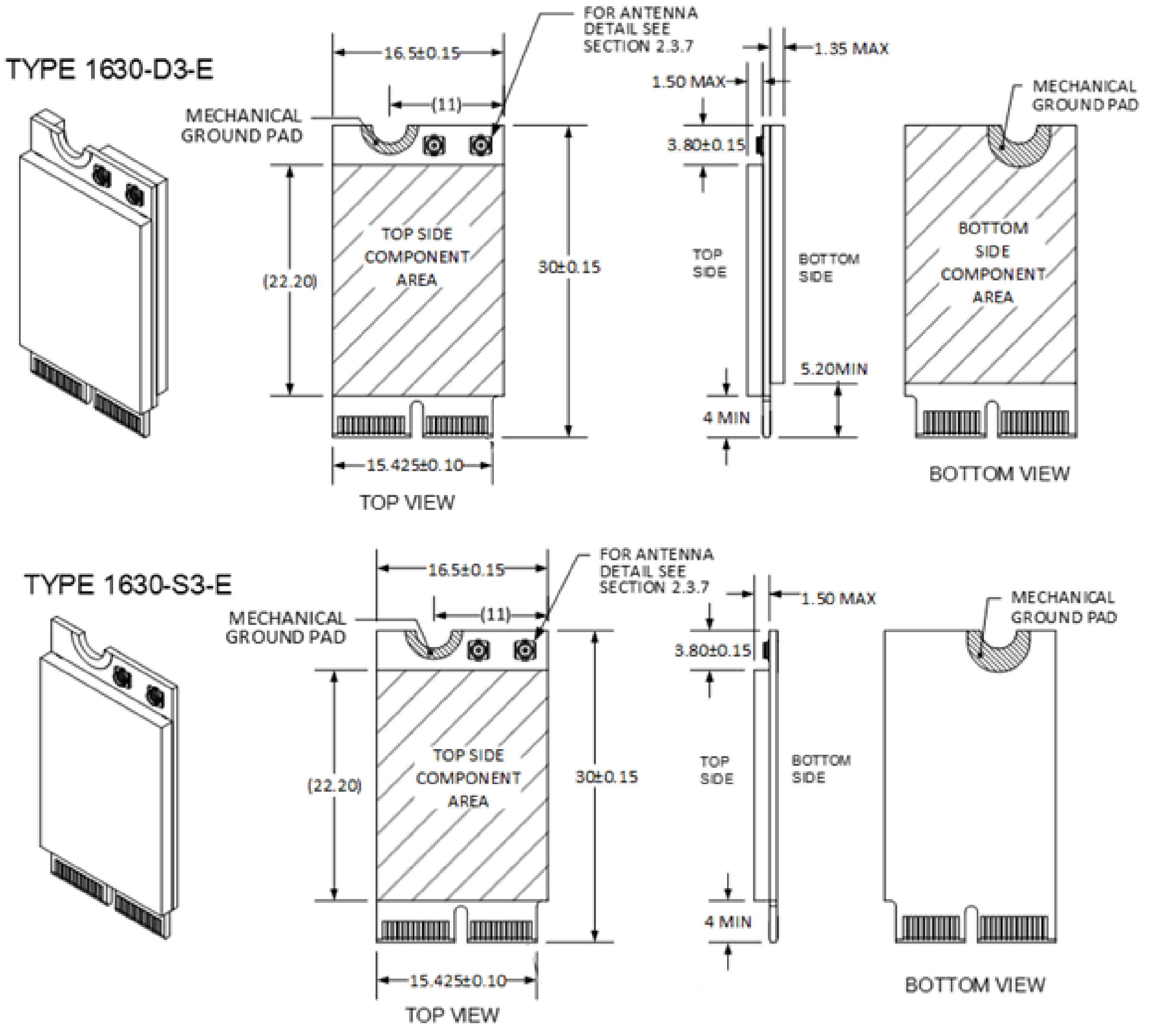
~~board/module~~ utilizes only the first 57 pin locations (a mechanical key uses 8 pins and the connector uses 49 pins for the host interface), it is limited in its connection capability.

Thus it is limited in the number of Comms that ~~can~~ are ~~be~~ simultaneously supported on ~~such a~~an Add-in Card~~board/module~~.

The mounting hole and the mechanical key are exactly the same as those in the Type 2230 so that the m~~M~~otherboard Socket ~~can support~~is capable of supporting both Type 2230 and Type 1630.

Note: ~~Board/module~~Add-in Card Type 1630 is limited to Key ID A ~~thru~~ through H only.

An example of the Type 1630 Add-in Card ~~board/module~~ mechanical outline drawing is shown in Figure 7.



Note: For card-edge details, see S~~S~~ection 2.3.4.~~, Card PCB Details~~

Figure 7. M.2 Type 1630-D3/S3 Mechanical Outline Drawing Examples

2.3.1.3. Type 3030 Specification

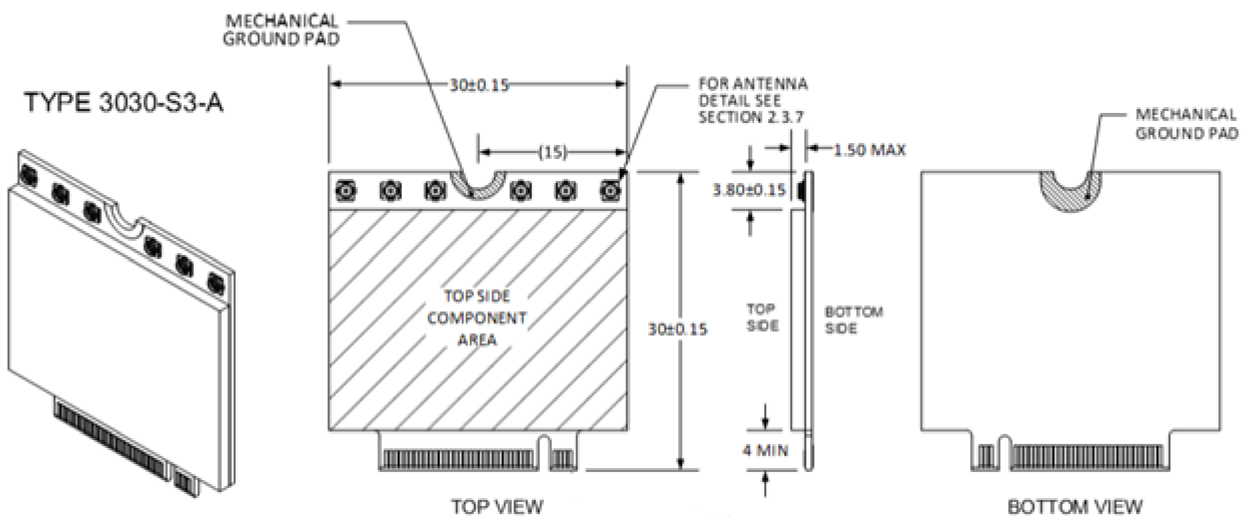
Type 3030 is an extended width M.2 Add-in Card ~~board/module~~ size used for more complex Comm combo solutions.

In principle the board is still comprised of three sections:

- Host ~~I/~~interface~~F~~ section
- RF connector and mounting hole section
- Active Component section

The active component section is 8 mm wider making an overall width of 30 mm (instead of the generic 22 mm width). The length remains the same at 30 mm so that it coincides with the other Type xx30 Add-in Cards~~boards/modules~~.

An example of the Type 3030 Add-in Card ~~board/module~~ mechanical outline drawing is shown in Figure 8. The wider board size will support a greater number of RF connectors. Up to six (6) RF connectors ~~can be~~are permitted to be populated while maintaining the recommended 4.5 mm center-to-center distances. See section 2.3.7, *RF Connectors* in this document for recommended locations and assignments.



Note: For card-edge details, see Section 2.3.4.~~section 2.3.4, Card PCB Details~~

Figure 8. M.2 Type 3030-S3 Mechanical Outline Drawing Example

2.3.2. Card Form Factors Intended for WWAN Socket 2

2.3.2.1. Type 3042 Specification

Type 3042 is an extended-width M.2 Add-in Card size used for WWAN solutions.

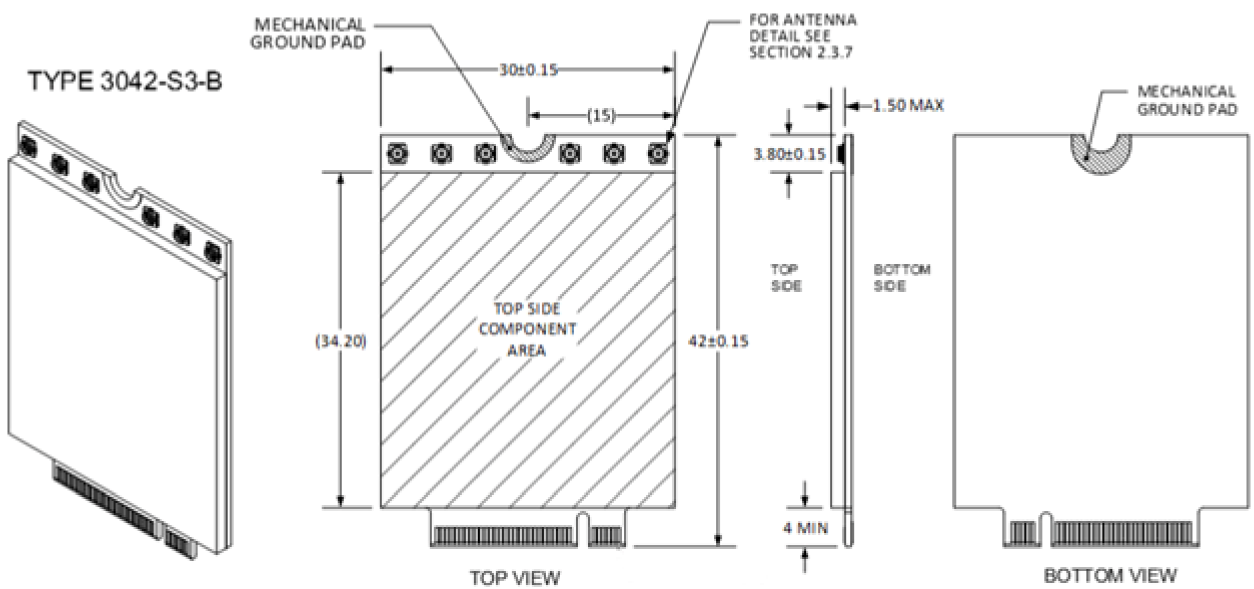
In principle the board is still comprised of three sections:

- Host interface~~I/F~~ section
- RF connector and mounting hole section
- Active Component section

The active component section is 8 mm wider making it wider than other Add-in Card alternatives intended for Socket 2 with the same overall length of 42 mm.

An example of the Type 3042 Add-in Card mechanical outline drawing is shown in Figure 9.

The wider board size will support a greater number of RF connectors. Up to six (6) RF connectors ~~can be~~are permitted to be populated while maintaining the recommended 4.5 mm center-to-center distances. See section 2.3.7, RF Connectors in this document for recommended locations and assignments.



Note: For card-edge details, see Section 2.3.4.~~section 2.3.4, Card PCB Details~~

Figure 9. M.2 Type 3042-S3 Mechanical Outline Drawing Example

2.3.2.2. Type 2242 Specification

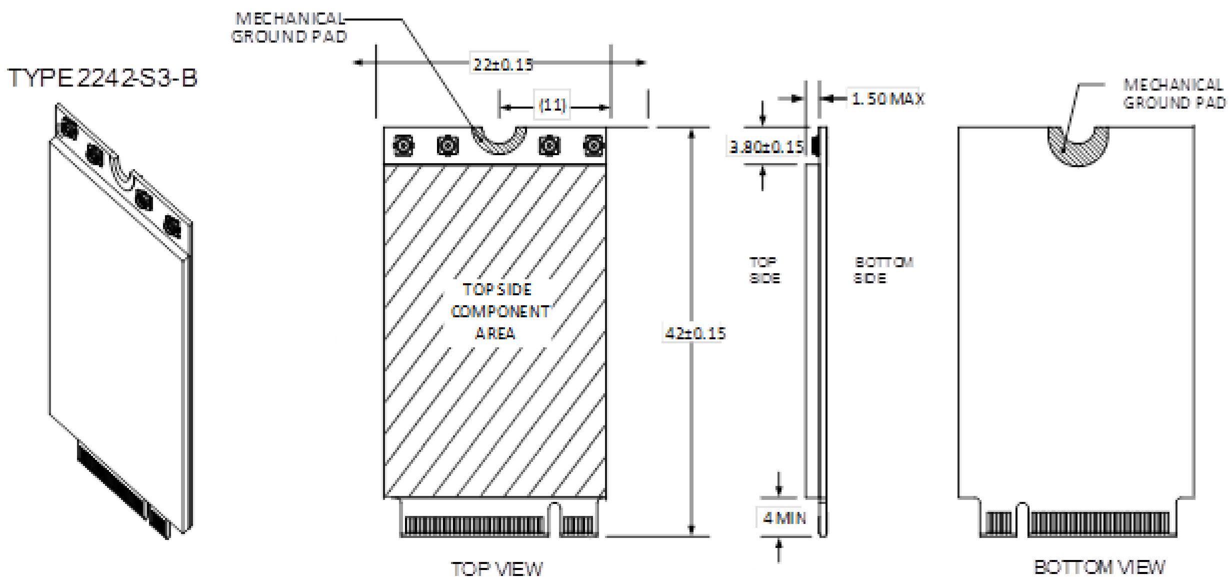
Type 2242 is an M.2 Add-in Card size used on Socket 2 and intended to support WWAN solutions. In principle the board is comprised of three sections:

- Host interface~~I/F~~ section
- RF connector and mounting hole section
- Active Component section

The active component section is 22 mm wide with the same overall length of 42 mm like the other Add-in Card intended for Socket 2.

An example of the Type 2242 Add-in Card mechanical outline drawing is shown in Figure 10.

The board size supports up to four (4) RF connectors~~, which can be~~ that are permitted to be populated while maintaining the recommended 4.5 mm center-to-center distances. See section 2.3.7 in this document for recommended locations and assignments.



Note: For card-edge details, see Section 2.3.4.~~section 2.3.4, Card PCB Details~~

Figure 10. M.2 Type 2242-S3 Mechanical Outline Drawing Example

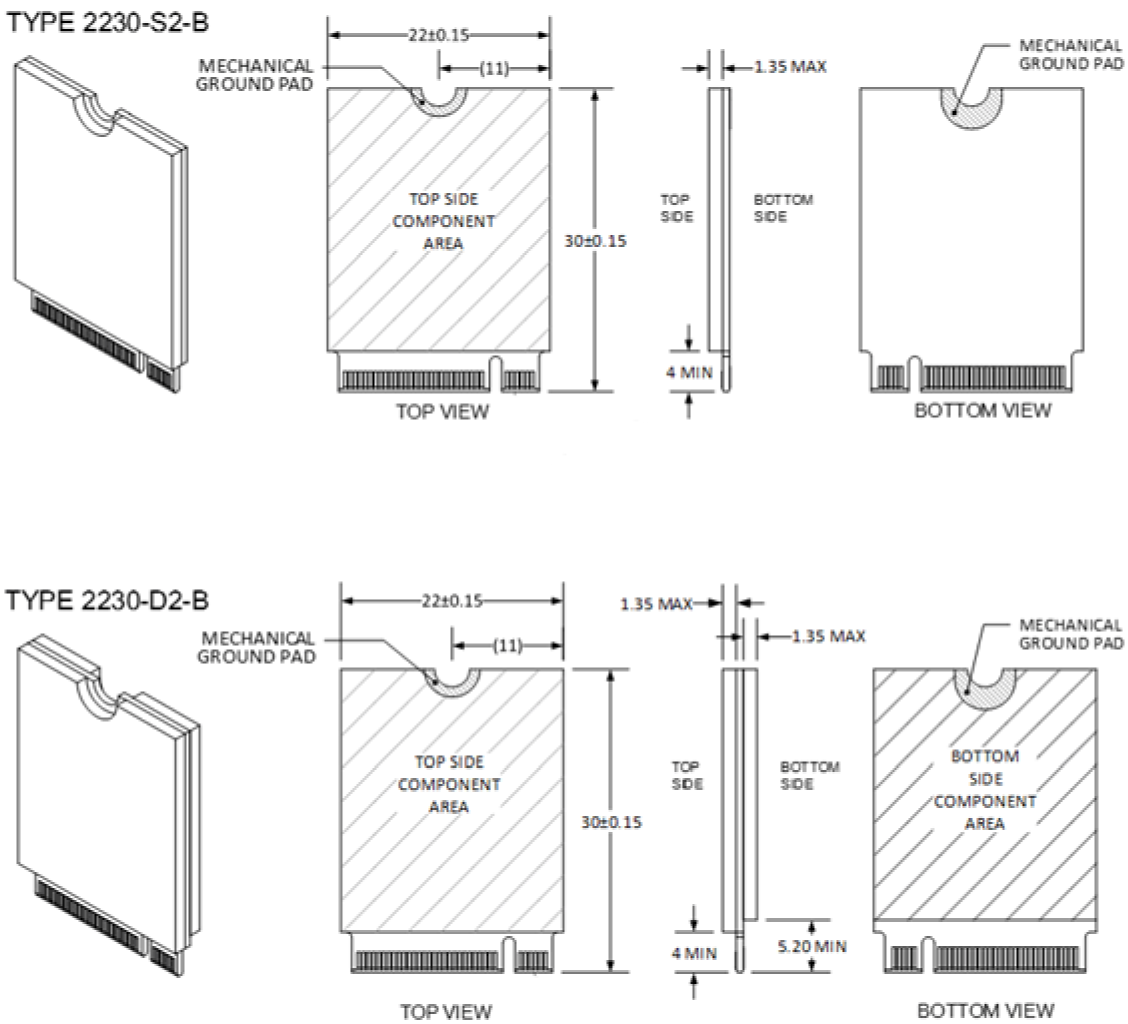
2.3.3. Card Form Factor for SSD Socket 2 and 3

2.3.3.1. Type 2230 Specification

Type 2230 is a M.2 Add-in Card size used on Socket 2 and Socket 3. It is intended to support SSD solutions and possibly other PCI Express-based solutions. The board is comprised of two sections:

- Host interface ~~I/F~~ section
- Active Component section

The active component section including the mounting-hole area has an overall length of 26 mm top-side and 24.8 mm bottom-side when applicable. Figure 11 shows Type 2230 Add-in Card mechanical outline drawing.



Note: For card-edge details, see Section 2.3.4.~~section 2.3.4, Card PCB Details~~

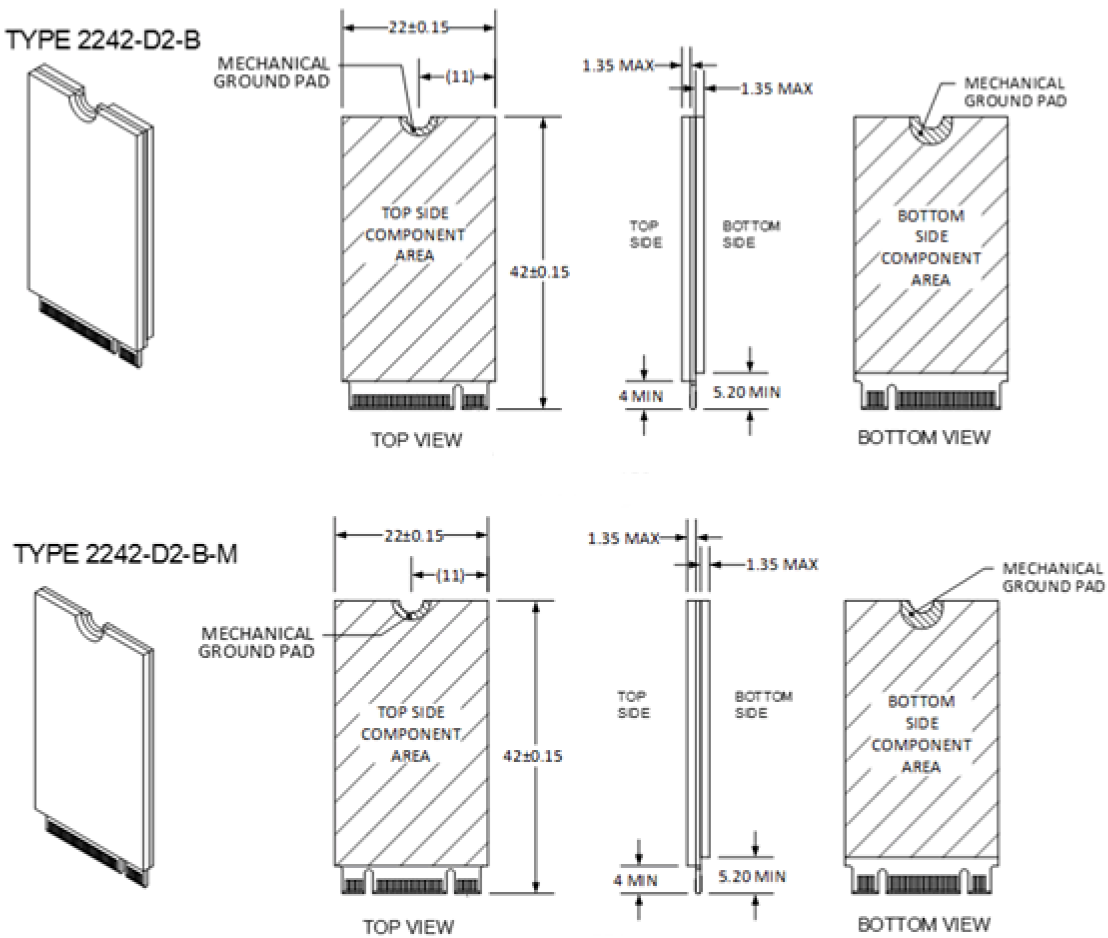
Figure 11. M.2 Type 2230-S2/D2 Mechanical Outline Drawing Examples

2.3.3.2. Type 2242 Specification

Type 2242 is a M.2 Add-in Card size used on Socket 2 and intended to support SSD solutions and possibly other PCI Express based solutions. In principle the board is still comprised of two sections:

- Host interface ~~I/F~~ section
- Active Component section

The active component section including the mounting hole area has an overall length of 38 mm top-side and 36.8 mm bottom side when applicable. Figure 12 shows Type 2242 Add-in Card mechanical outline drawing. The SSD Add-in Card ~~can~~ takes advantage of the Dual Add-in Card key scheme to enable this Add-in Card to plug into two different SSD-capable Sockets (~~for example~~e.g., Socket 2 and Socket 3).

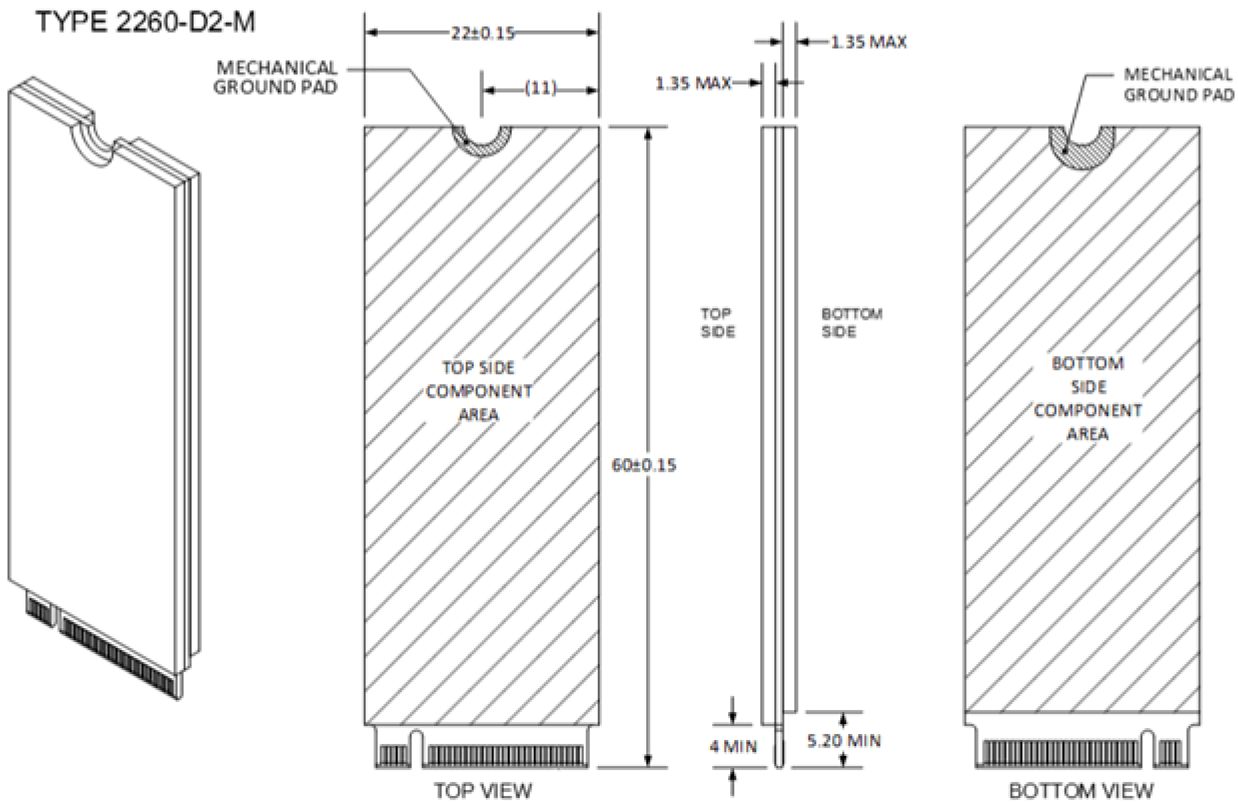


Note: For card-edge details, see Section 2.3.4.~~section 2.3.4, Card PCB Details~~

Figure 12. M.2 Type 2242-D2 Mechanical Outline Drawing Top-side Examples

2.3.3.3. Type 2260 Specification

Type 2260 Add-in Card is primarily intended to support high capacity SSD solutions. Figure 13 shows an example of Type 2260.

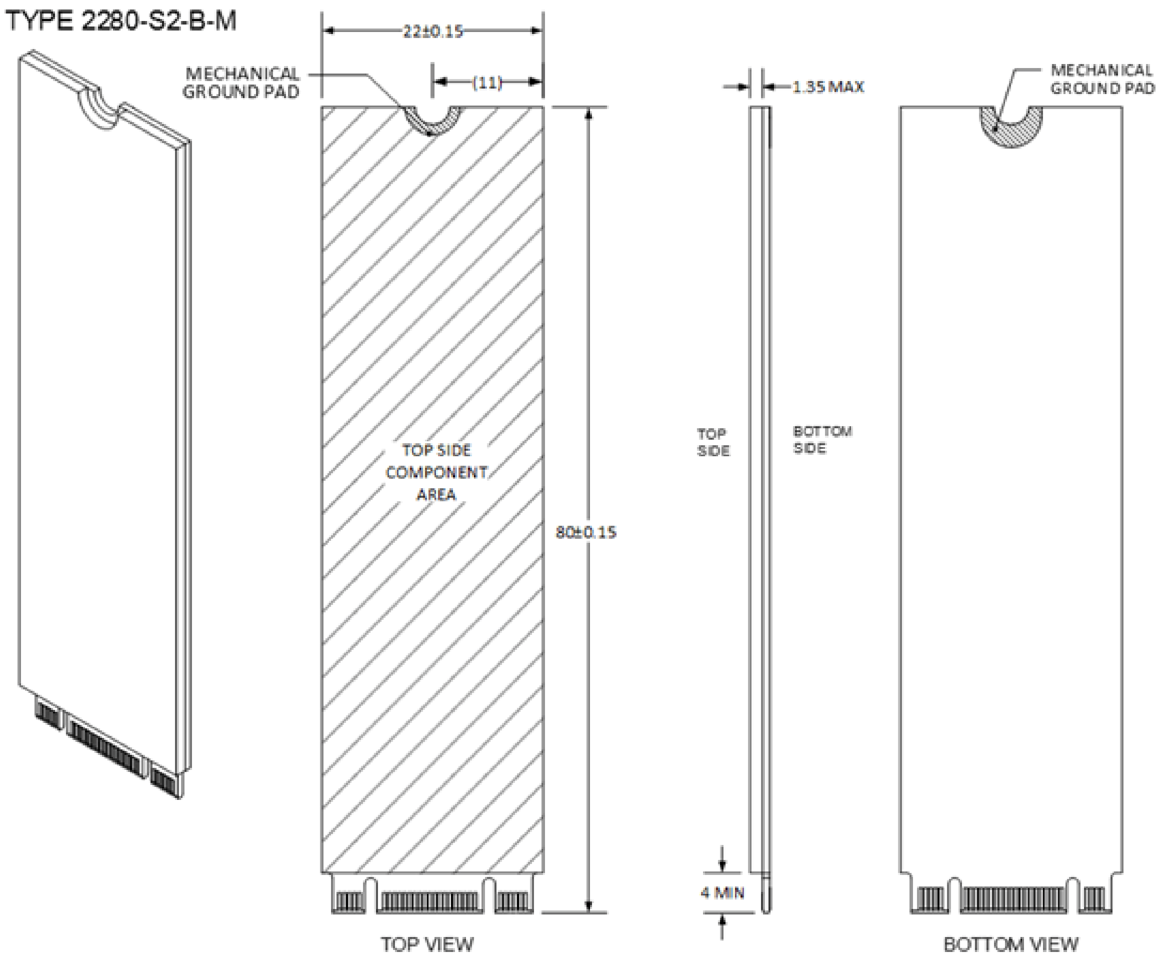


Note: For card-edge details, see Section 2.3.4.~~section 2.3.4, Card PCB Details~~

Figure 13. M.2 Type 2260-D2 Mechanical Outline Drawing Example

2.3.3.4. Type 2280 Specification

This Add-in Card type is primarily intended to support high-capacity SSD solutions. Figure 14 shows an example of Type 2280.

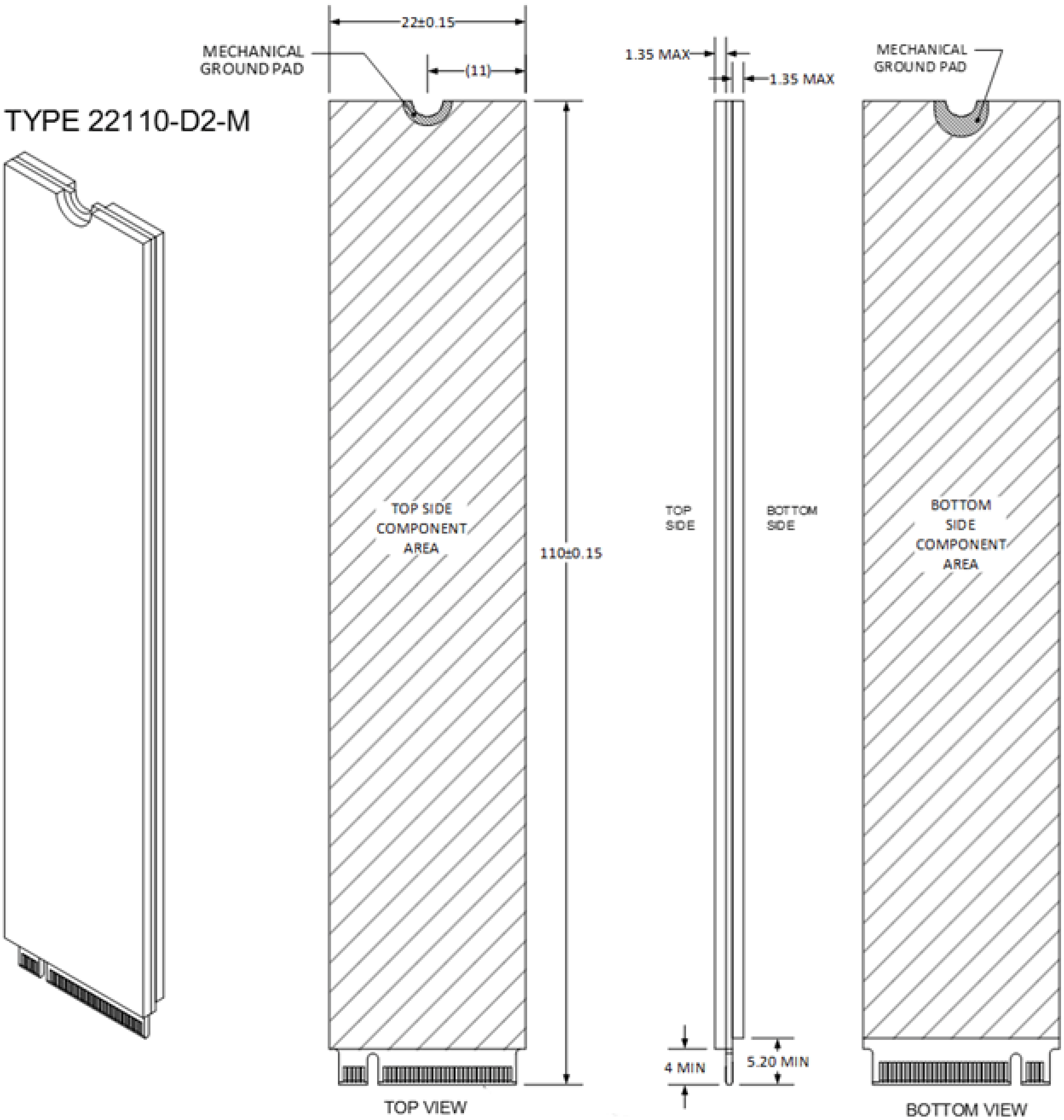


Note: For card-edge details, see Section 2.3.4~~.section 2.3.4, Card PCB Details~~

Figure 14. M.2 Type 2280-S2 Mechanical Outline Drawing Example

2.3.3.5. Type 22110 Specification

This Add-in Card type is primarily intended to support high-capacity SSD solutions. Figure 15 shows an example of Type 22110.



Note: For card-edge details, see Section 2.3.4.~~section 2.3.4, Card PCB Details~~

Figure 15. M.2 Type 22110-D2 Mechanical Outline Drawing Example

2.3.4. Card PCB Details

2.3.4.1. Mechanical Outline of Card-Edge

Figure 16, Figure 17, and Figure 18 show typical card-edge mechanical outlines.

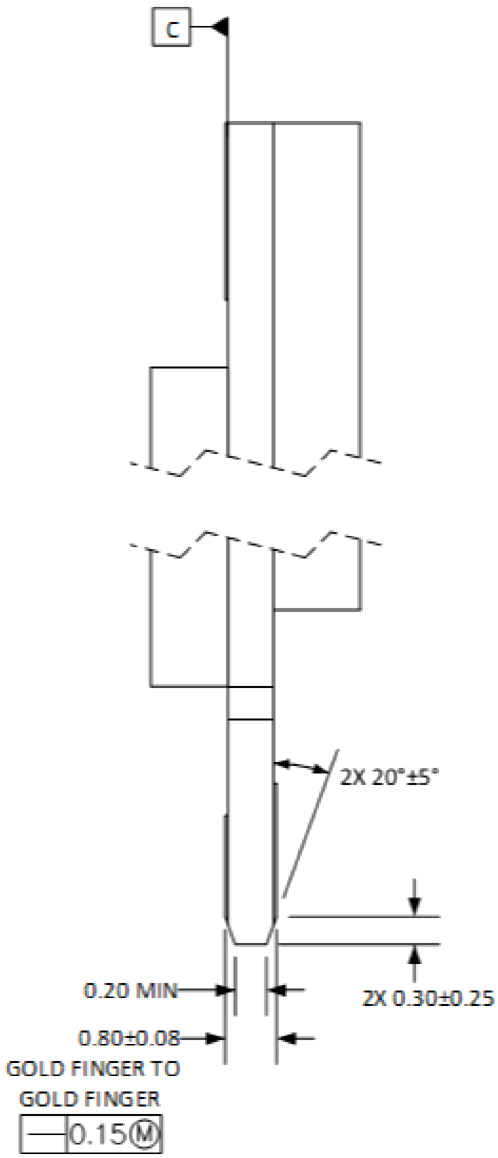
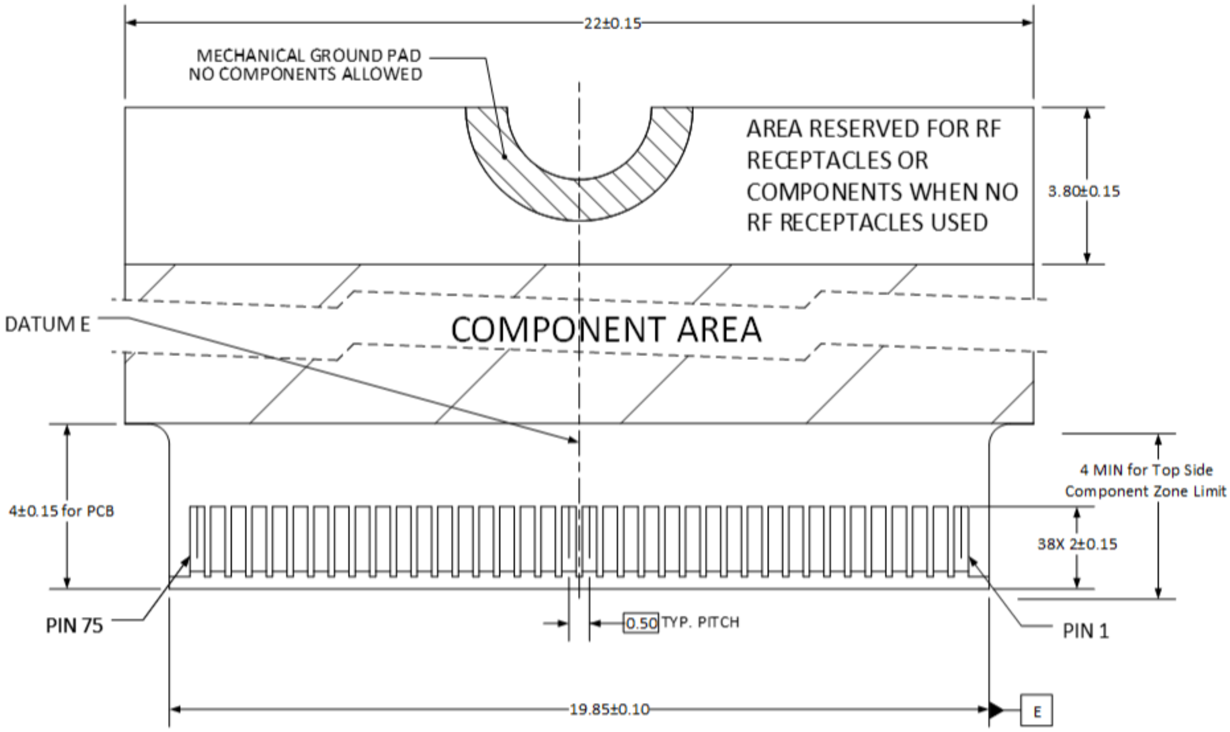
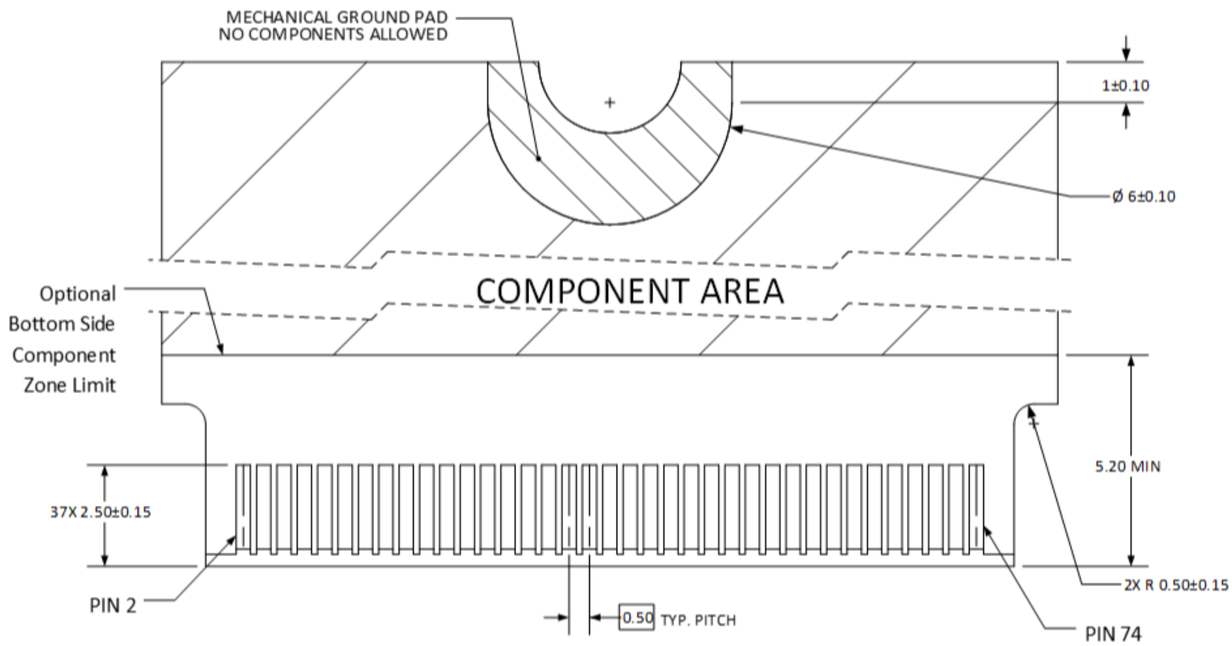


Figure 16. Card Edge Bevel

382 

383 Figure 17. Card Edge Outline Top-side

384 

385 Figure 18. Card Edge Outline Bottom-side

386

2.3.4.2. Add-in Card Keying

Note: ~~–~~Key G is shown for reference only! This Key is allocated for custom use at one's own risk. It is not used for M.2 spec compliant devices.

Keying is required to provide configurability as well as preventing incompatible Add-in Card insertion. See the following figures and tables for dimensional values.

- Table 3. Key Location/Pin Block Dimensions for Keys A to F
- ~~Table 3. Key Location/Pin Block Dimensions for Keys A - F~~
- Table 4. Key Location/Pin Block Dimensions for Keys G to M~~Table 4. Key Location/Pin Block Dimensions for Keys G - M~~
- Figure 19. Key Detail for Keys A to F
- ~~Figure 19. Key Detail for Keys A Thru F~~
- ~~Figure 20. Key Detail for Keys G Thru M~~Figure 20. Key Detail for Keys G to M
- Figure 21. Dual Key A-E Example
- Figure 22. Dual Key B-M Example

The key locations and pin block dimensions for Keys A to F are listed in Table 3~~Table 3~~. Table 4~~Table 4~~ lists Keys G to M~~-~~. The key designation identifier should be marked with either Silk Screen, reverse copper etching, or solder mask removal on the Top-side of the Add-in Card to the right of the
Add-in Card key, as shown in Figure 19 and Figure 20. The letter size should be at least 1 mm tall.

Table 3. Key Location/Pin Block Dimensions for Keys A ~~-~~to F

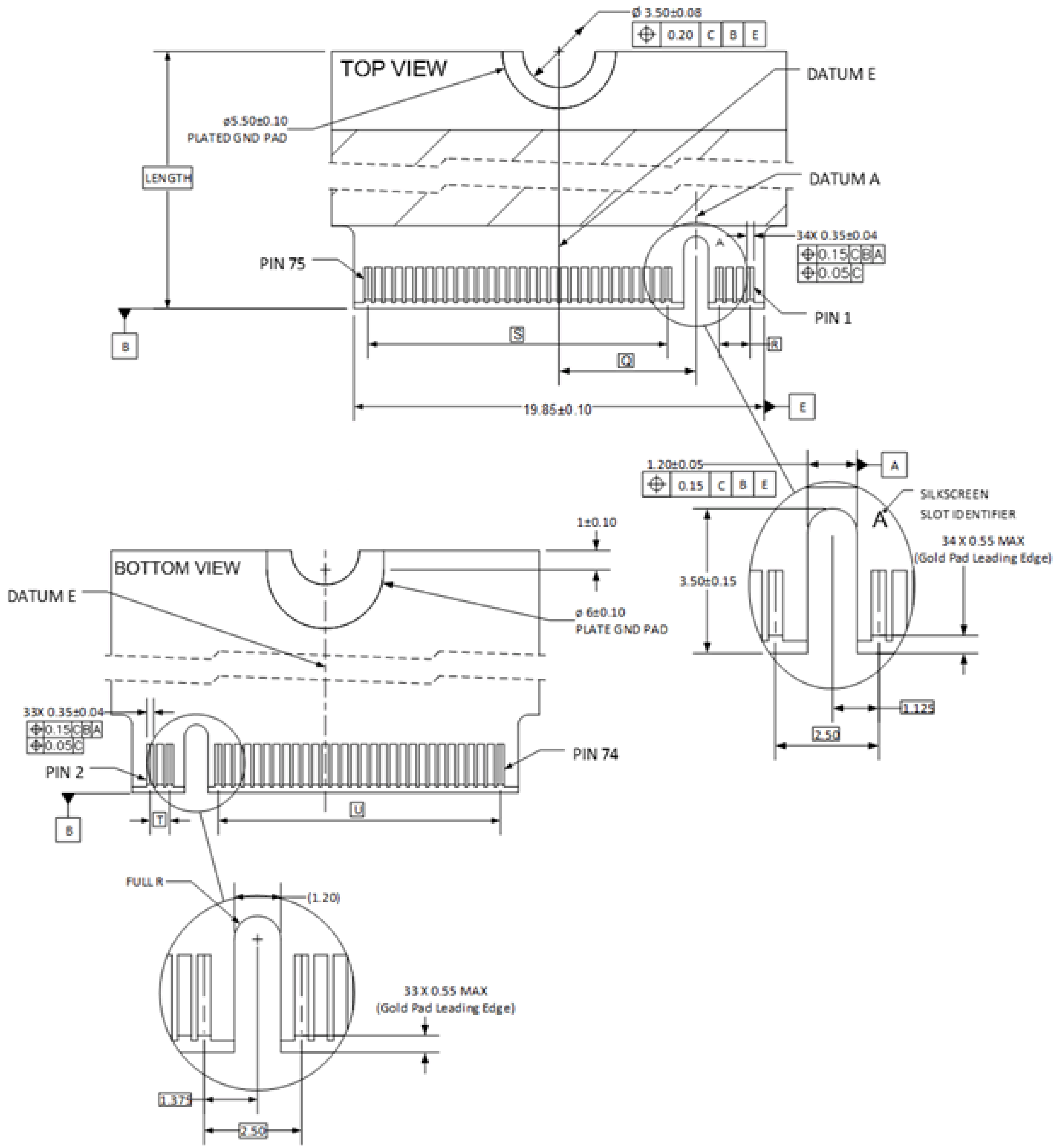
Dimension	Key ID A	B	C	D	E	F
Q	6.625	5.625	4.625	3.625	2.625	1.625
R	1.50	2.50	3.50	4.50	5.50	6.50
S	14.50	13.50	12.50	11.50	10.50	9.50
T	1.00	2.00	3.00	4.00	5.00	6.00
U	14.50	13.50	12.50	11.50	10.50	9.50

Table 4. Key Location/Pin Block Dimensions for Keys G ~~-~~to M

Dimension	Key ID G	H	J	K	L	M
V	1.125	2.125	3.125	4.125	5.125	6.125
W	9.00	10.00	11.00	12.00	13.00	14.00
X	7.00	6.00	5.00	4.00	3.00	2.00

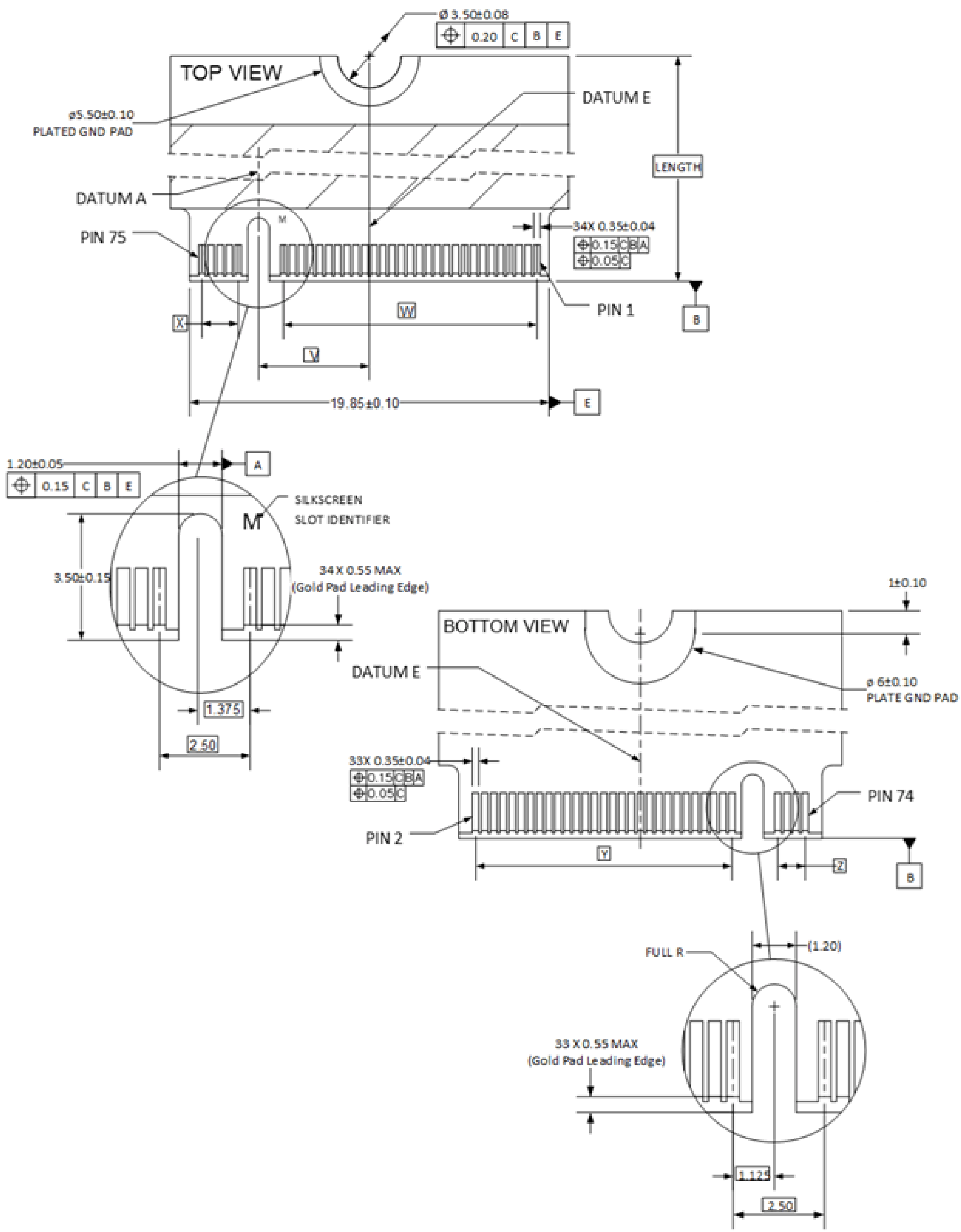
Y	9.00	10.00	11.00	12.00	13.00	14.00
Z	6.50	5.50	4.50	3.50	2.50	1.50

Two Key designation identifiers should be marked when the Add-in Card employs a dual Add-in Card key scheme as shown in Figure 20 ~~Figure 20~~ and Figure 21~~Figure 21~~ respectively.



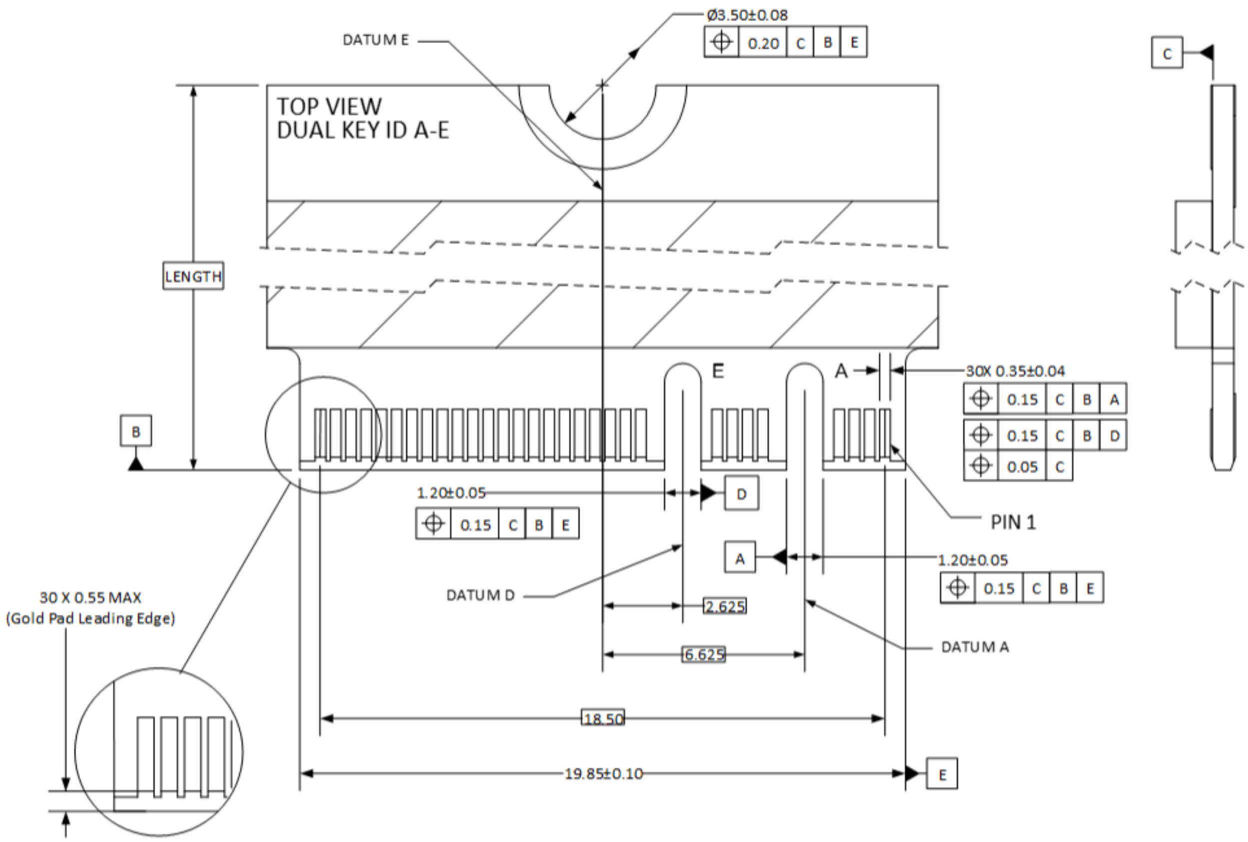
Note: See Figure 3 for LENGTH

Figure 19. Key Detail for Keys A ~~Thru~~ to F



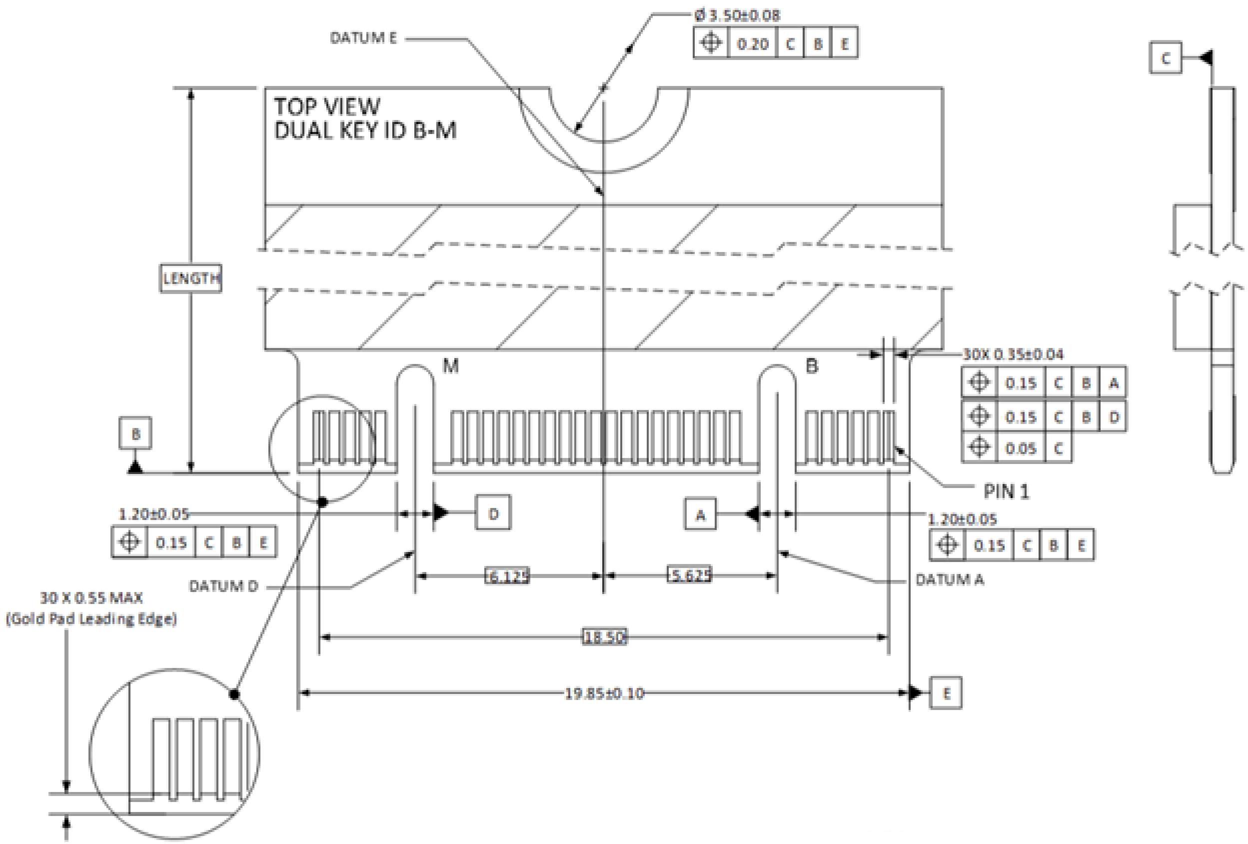
Note: See Figure 3 for LENGTH

Figure 20. Key Detail for Keys G ~~Thru~~ to M



Note: See Figure 3 for LENGTH

Figure 21. Dual Key A-E Example



Note: See Figure 3 for LENGTH

Figure 22. Dual Key B-M Example

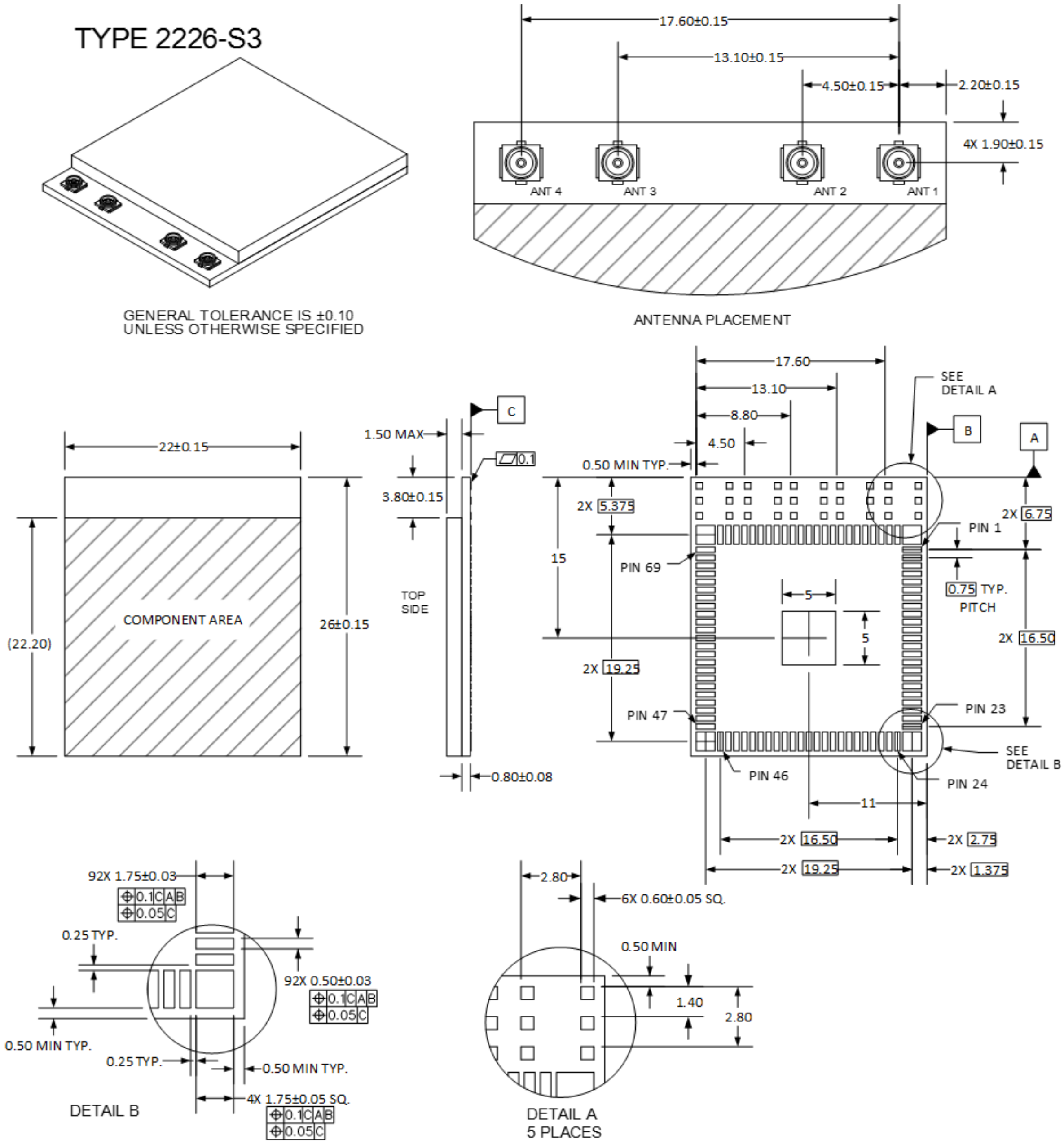
2.3.5. Soldered-down Form Factors

2.3.5.1. Type 2226 Specification

Type 2226 Module is a soldered-down, single-sided version of Type 2230 Add-in Card. It is therefore assuming the same board technology and silicon package technology. It has an LGA land pattern on the backside instead of the 75 position Host Interface Edge Card gold finger connector. As a result of this, Type 2226 is 4 mm shorter.

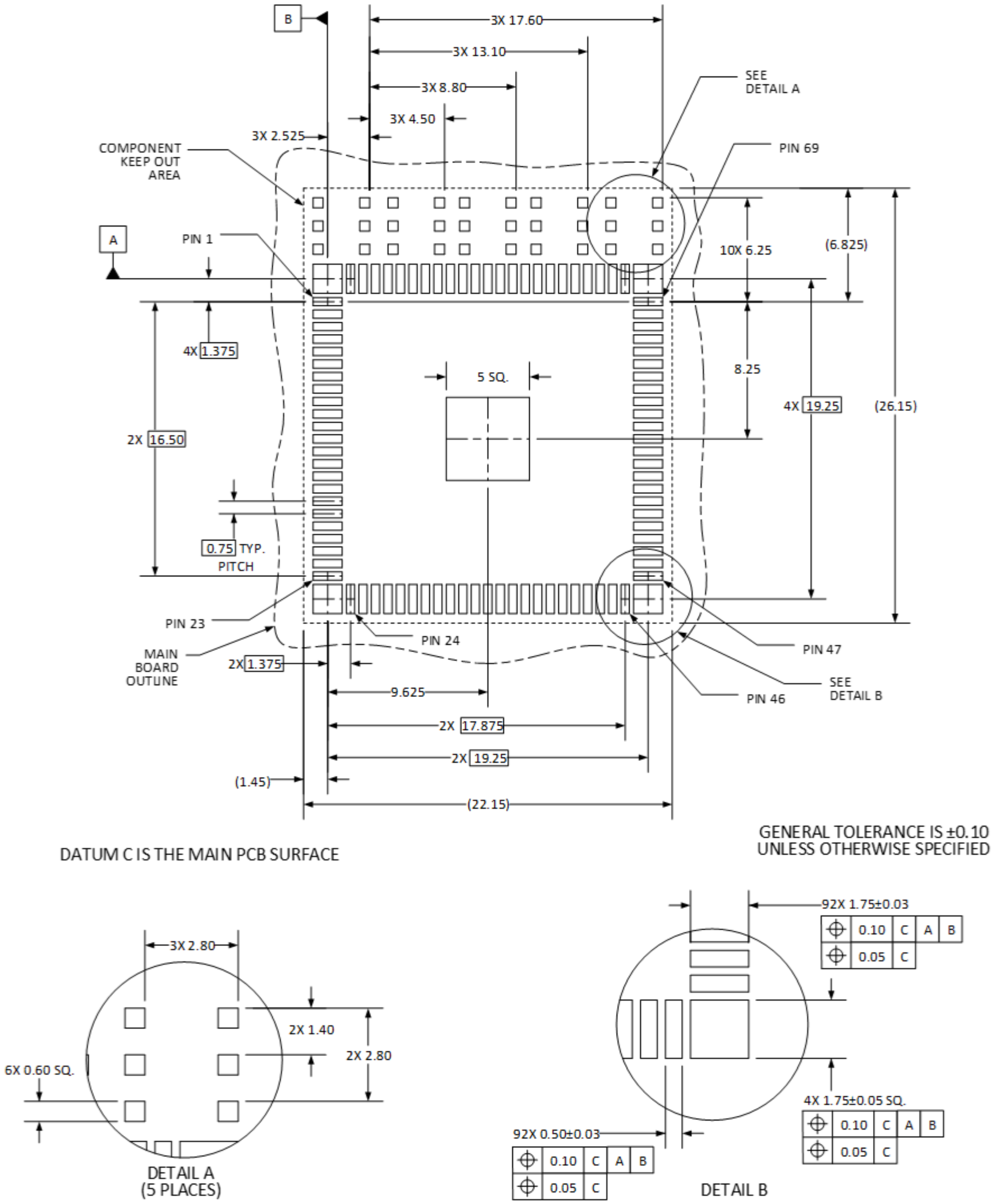
To help prevent PCB-warp, it is recommended to balance the copper area of the PCB layers. The guideline recommendation is for the difference between copper area of mirrored layers (e.g~~i.e~~., outer to outer layer, first inner on top to first inner on bottom, etc.) to be equal to or less than 15%.

Figure 23 shows the mechanical outline drawing for Module Type 2226. The recommended land pattern is given in Figure 24.

436 

437 Figure 23. M.2 Type 2226-S3 Mechanical Outline Drawing Example

438



439

440 Figure 24. Recommended Land Pattern for Module Type 2226

2.3.5.2. Type 1216 Specification

This Module type is another single-sided soldered-down solution based on a higher density interconnect technology and a smaller silicon package technology. It has an LGA land pattern on the backside and therefore the size is smaller.

To help prevent PCB-warp, it is recommended to balance the copper area of the PCB layers. The guideline recommendation is for the difference between copper area of mirrored layers (~~for example~~e.g., outer to outer layer, first inner on top to first inner on bottom, etc.) to be equal to or less than 15%.

Figure 25 shows the mechanical outline drawing for Module Type 1216. The recommended land pattern is given in Figure 26.

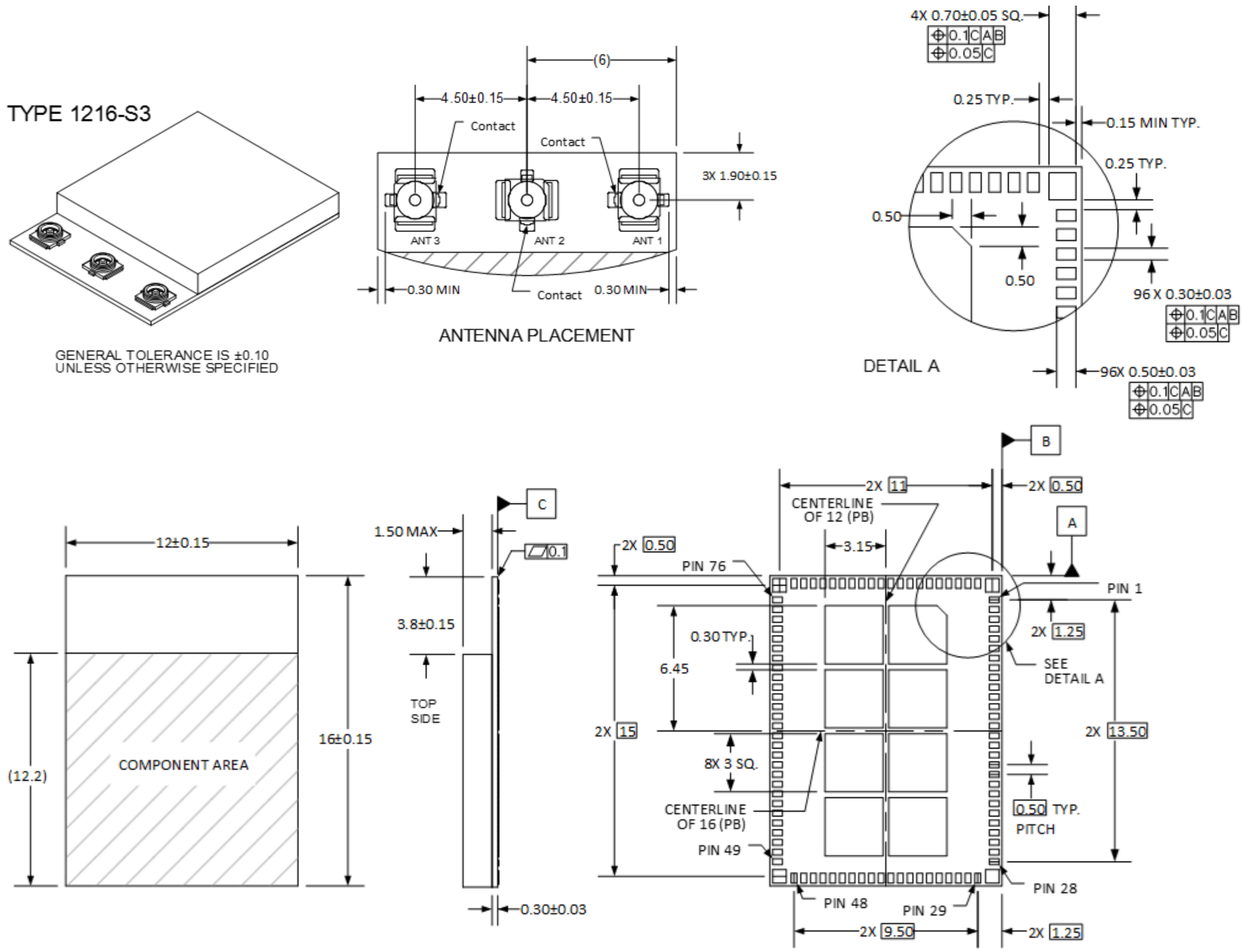
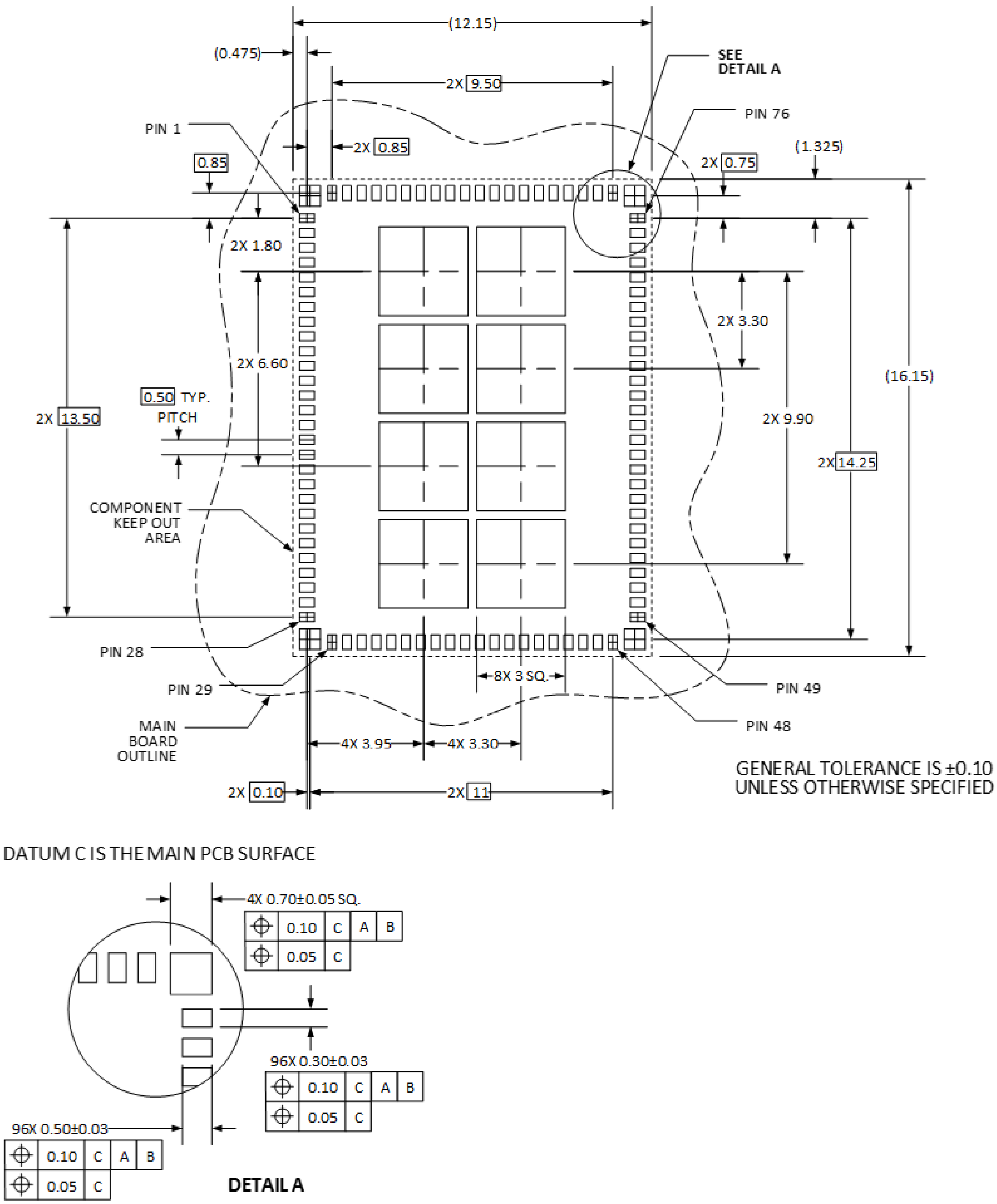


Figure 25. M.2 Type 1216-S3 Mechanical Outline Drawing Example



455

456 Figure 26. Recommended Land Pattern for Module Type 1216

2.3.5.3. Type 3026 Specification

This Module type is a single-sided soldered-down version of the Type 3030 Add-in Card and assumes the same board and silicon package technology. It has a unique LGA land pattern on the backside instead of the 75 position Host Interface Edge Card gold finger connector. This LGA pattern ~~can~~ accommodates a Type 2226 Module as a drop-in replacement located at the center with two sets of LGA pads along the sides that cover the entire 3026 Module size. Like the Type 2226 Module, the Module size is also 4 mm shorter than the Add-in Card version.

To help prevent the Module from warping, it is recommended to balance the copper area of the PCB layers. The guideline recommendation is for the difference between copper area of mirrored layers (~~for example~~e.g.~~;~~, outer-to-outer layer, first inner on top to first inner on bottom, etc.) to be equal to or less than 15%.

Figure 27 shows the mechanical outline drawing for Module Type 3026. See Figure 28 for more detailed information. The recommended land pattern is given in Figure 29.

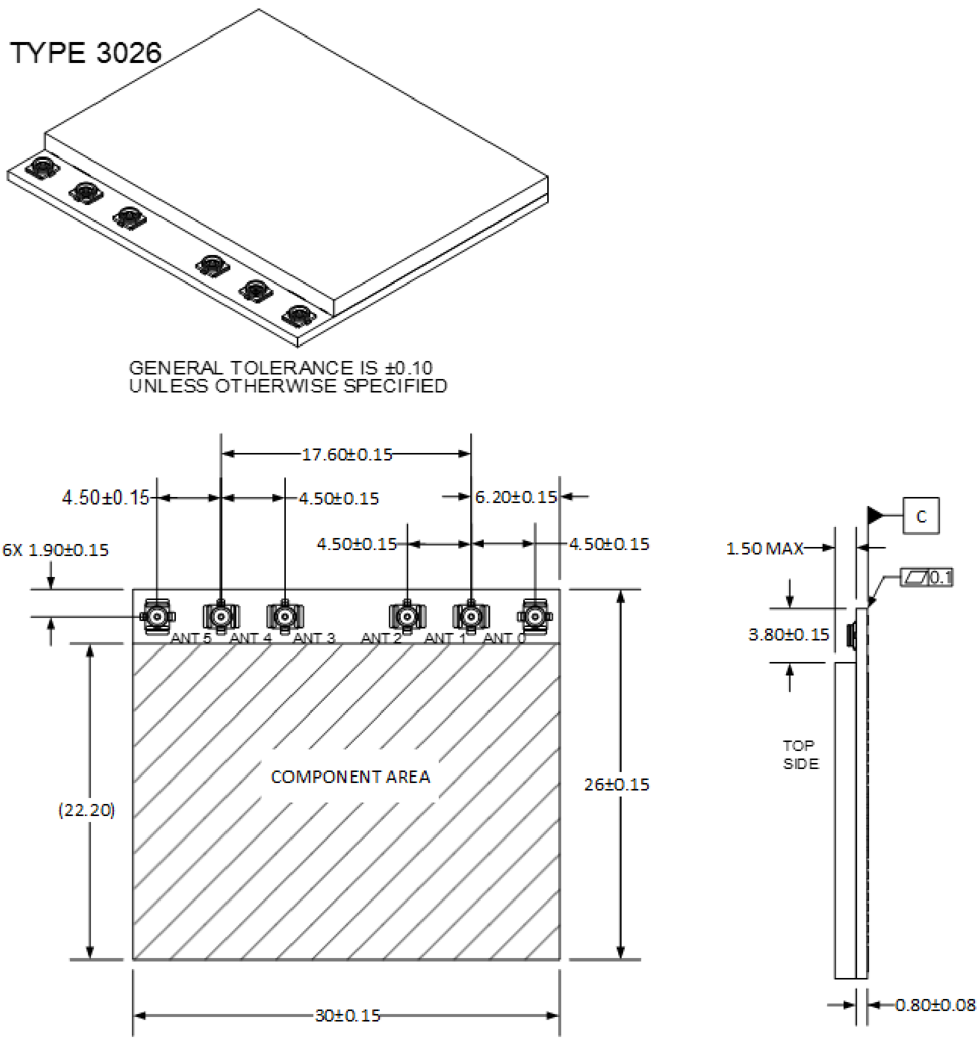


Figure 27. M.2 Type 3026-S3 Mechanical Outline Drawing Example

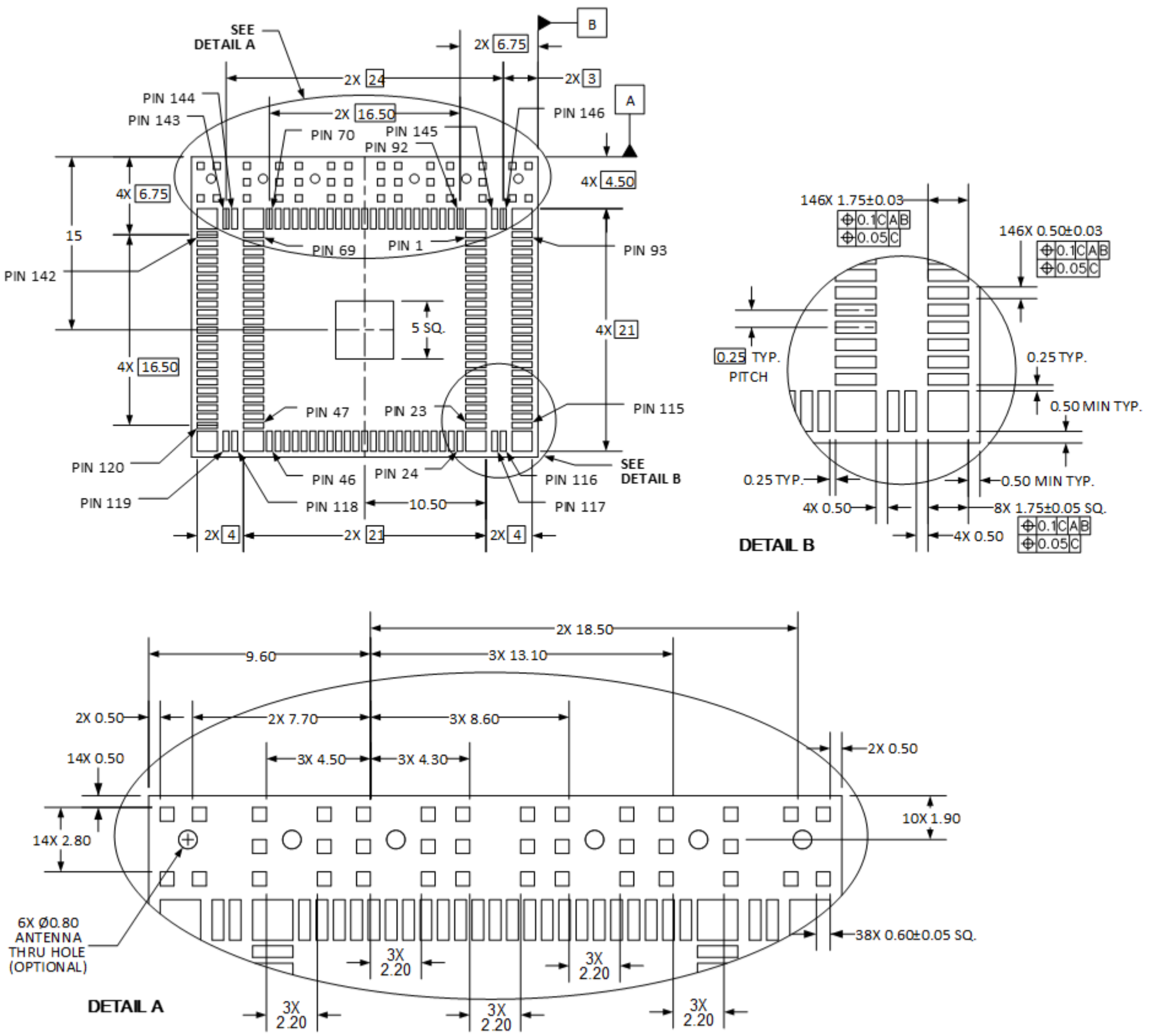
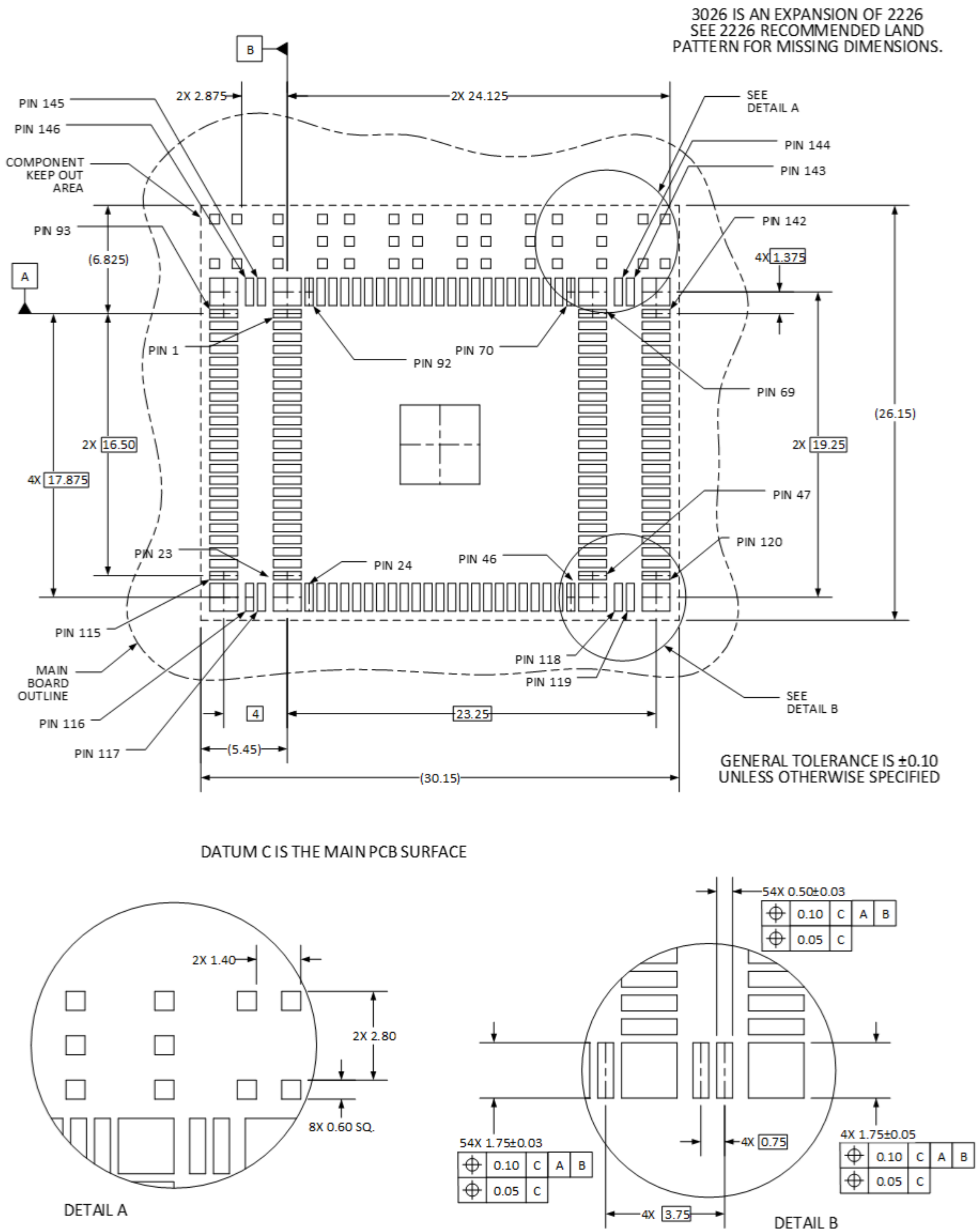


Figure 28. M.2 Type 3026-S3 Mechanical Outline Drawing Details Example



476

477 Figure 29. Recommended Land Pattern for M.2 Type 3026

2.3.6. Soldered-Down Form Factors for BGA SSDs

Following different sizes are defined for the soldered-down BGA SSDs:

- Type 1620
- Type 2024
- Type 2228
- Type 2828

All these types are soldered-down and single-sided. They have a BGA land pattern on the backside.

To help prevent PCB-warp, it is recommended to balance the copper area of the PCB layers. The guideline recommendation is for the difference between copper area of mirrored layers (~~for example~~e.g., outer-to-outer layer, first inner on top to first inner on bottom, etc.) to be equal to or less than 15%.

The target differential impedance of the PCIe and SATA signals on the package is 85 Ω. Differential coupling from other signals must be reduced to ensure signal integrity of the differential pair.

2.3.6.1. Type 1620 Specification

BGA package sizes of 2024, 2228, and 2828 contain the common core ball map of Type 1620. The larger packages of Type 2024, Type 2228, and Type 2828 have retention balls in addition to the core Type 1620 ball map.

Figure 30 shows the mechanical outline drawing for BGA Type 1620 and Figure 31 shows a recommended land pattern for Type 1620 package. The dimensions shown in Figure 31 are nominal.

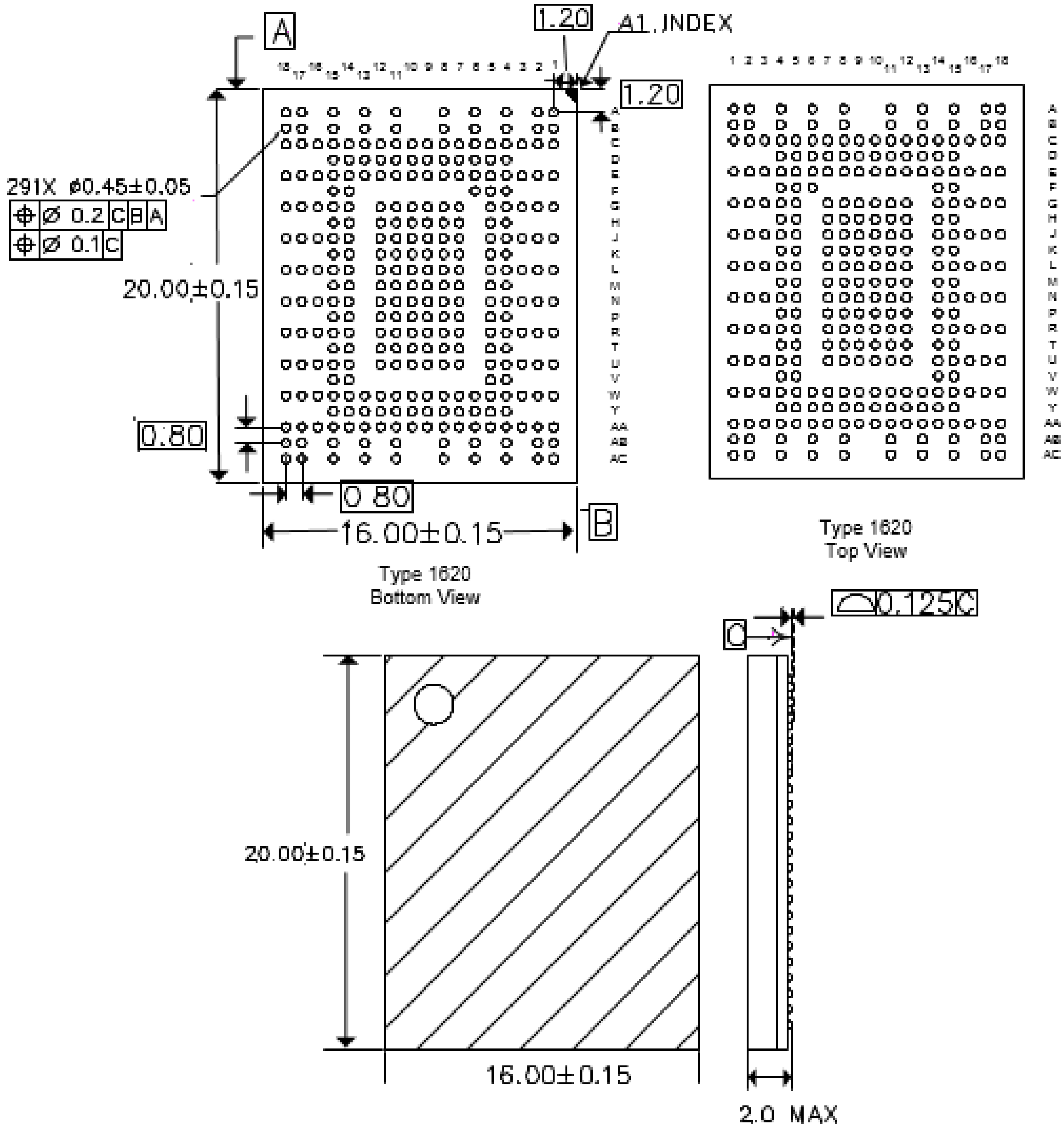


Figure 30. M.2 Type 1620-S5 Mechanical Outline Drawing Example

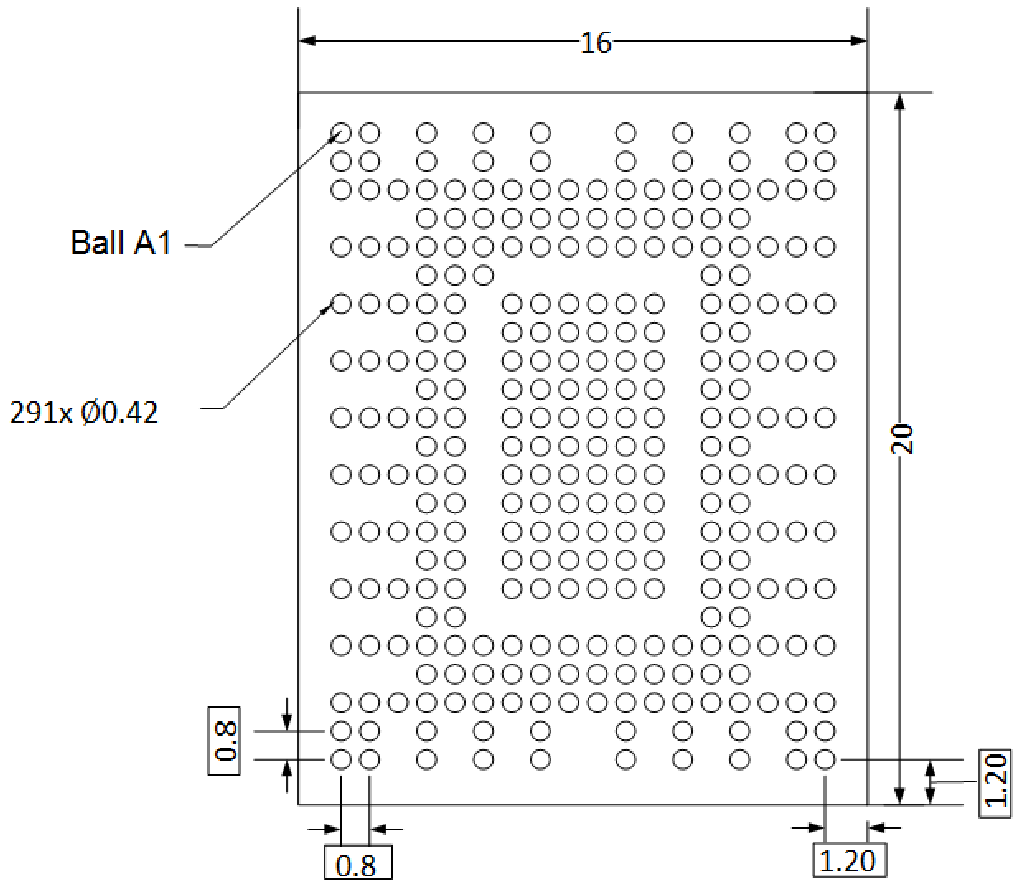


Figure 31. Recommended Land Pattern for M.2 Type 1620 BGA (Top View)

2.3.6.2. Type 2024 Specification

Figure 32 shows an example of the M.2 Type 2024-S5 mechanical outline drawing and Figure 33 shows a recommended land pattern for the Type 2024 package (dimensions shown in this figure are nominal).

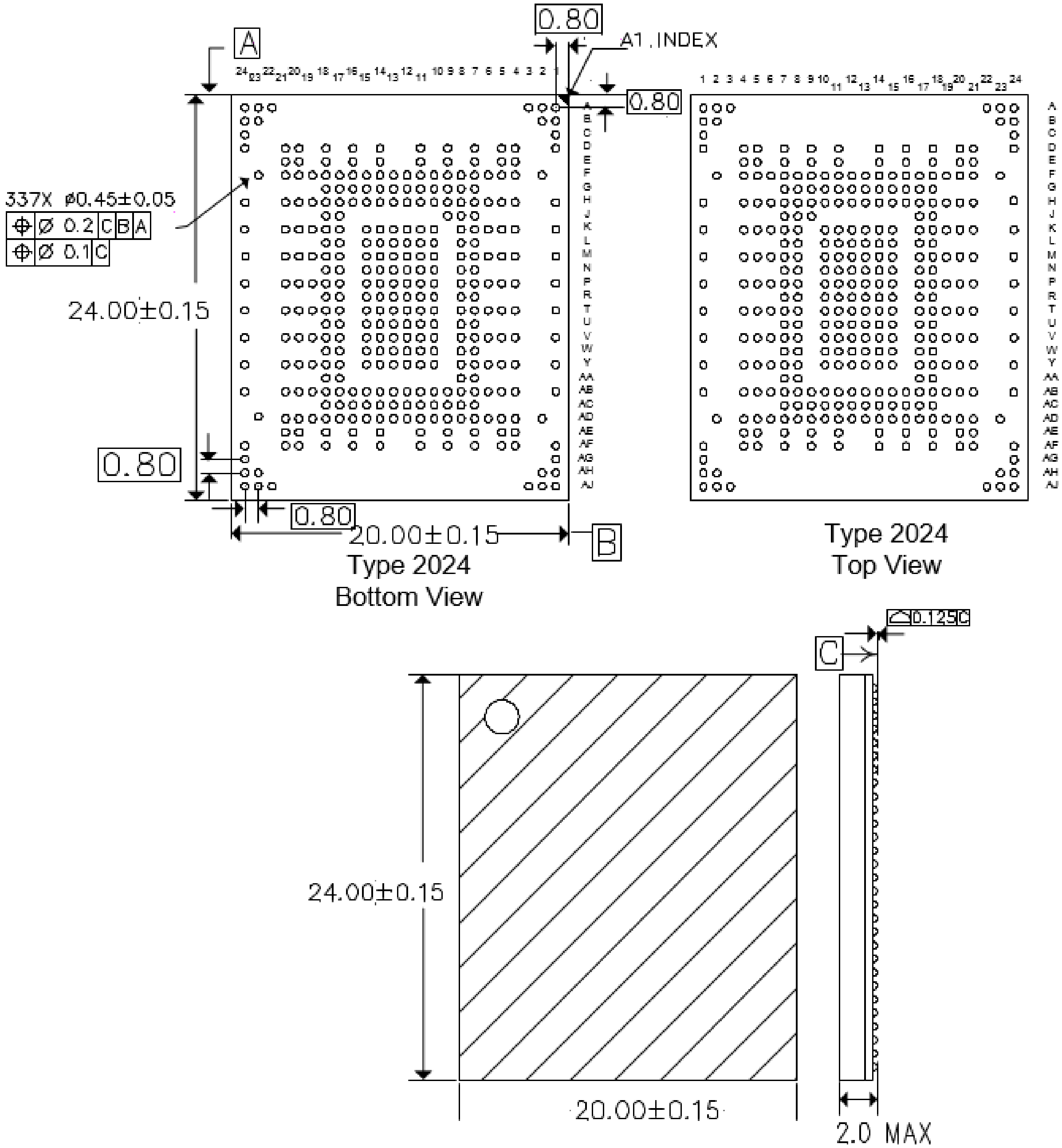


Figure 32. M.2 Type 2024-S5 Mechanical Outline Drawing Example

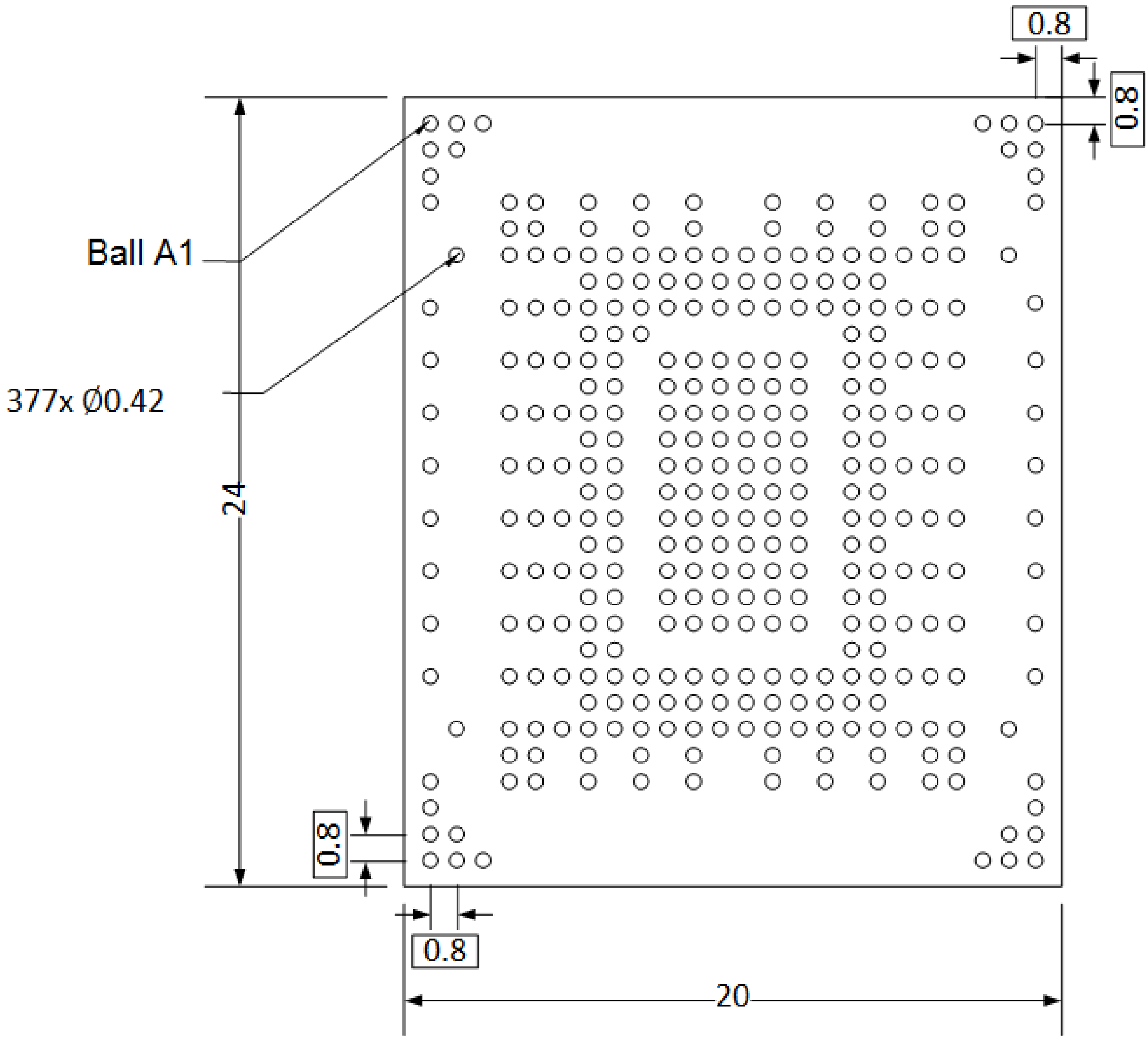


Figure 33. Recommended Land Pattern for M.2 Type 2024 BGA (Top View)

2.3.6.3. Type 2228 Specification

Figure 34 shows an example of the M.2 Type 2228-S5 mechanical outline drawing and Figure 35 shows the recommended land pattern for Type 2228 package (dimensions shown in this figure are nominal).

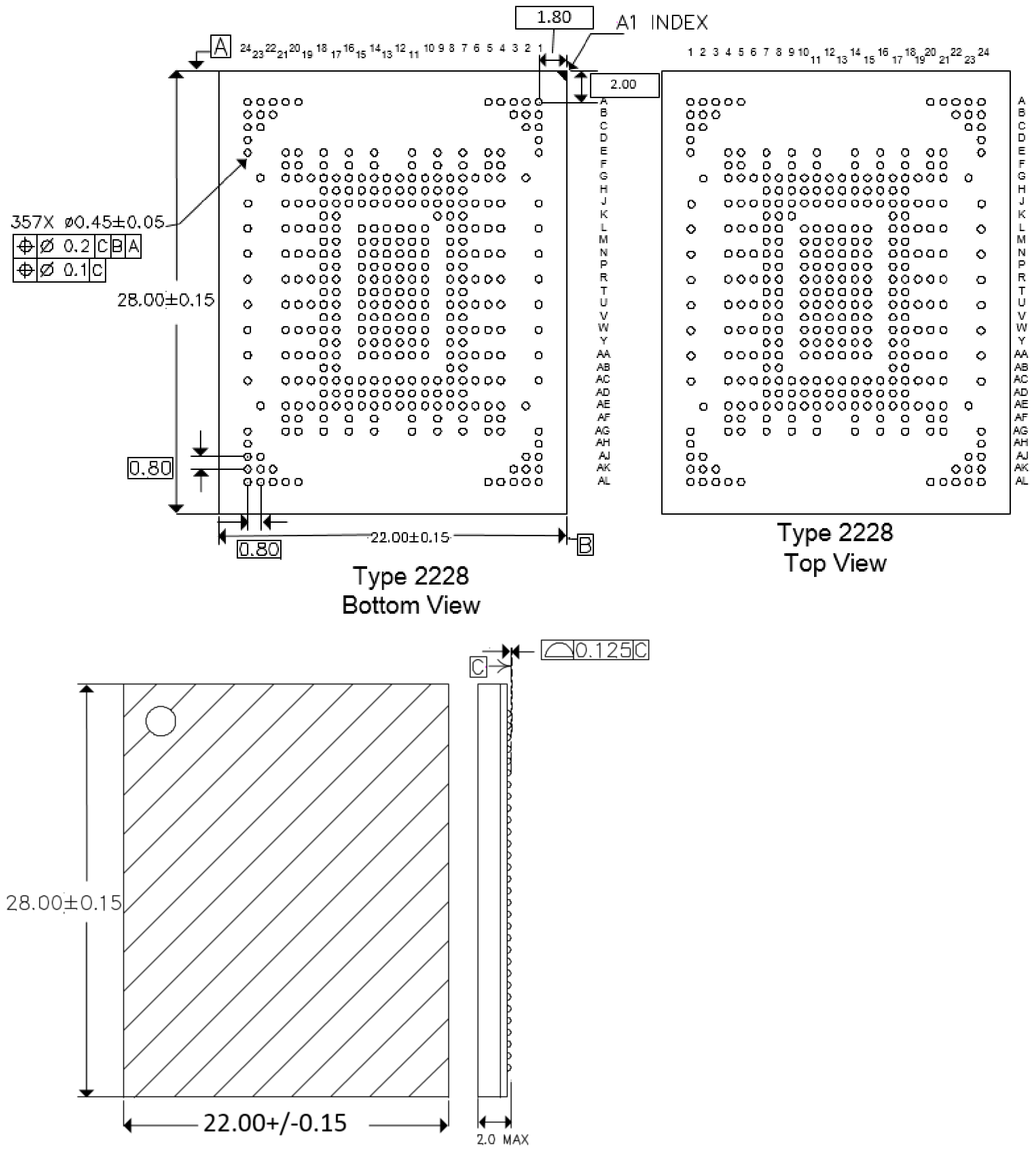
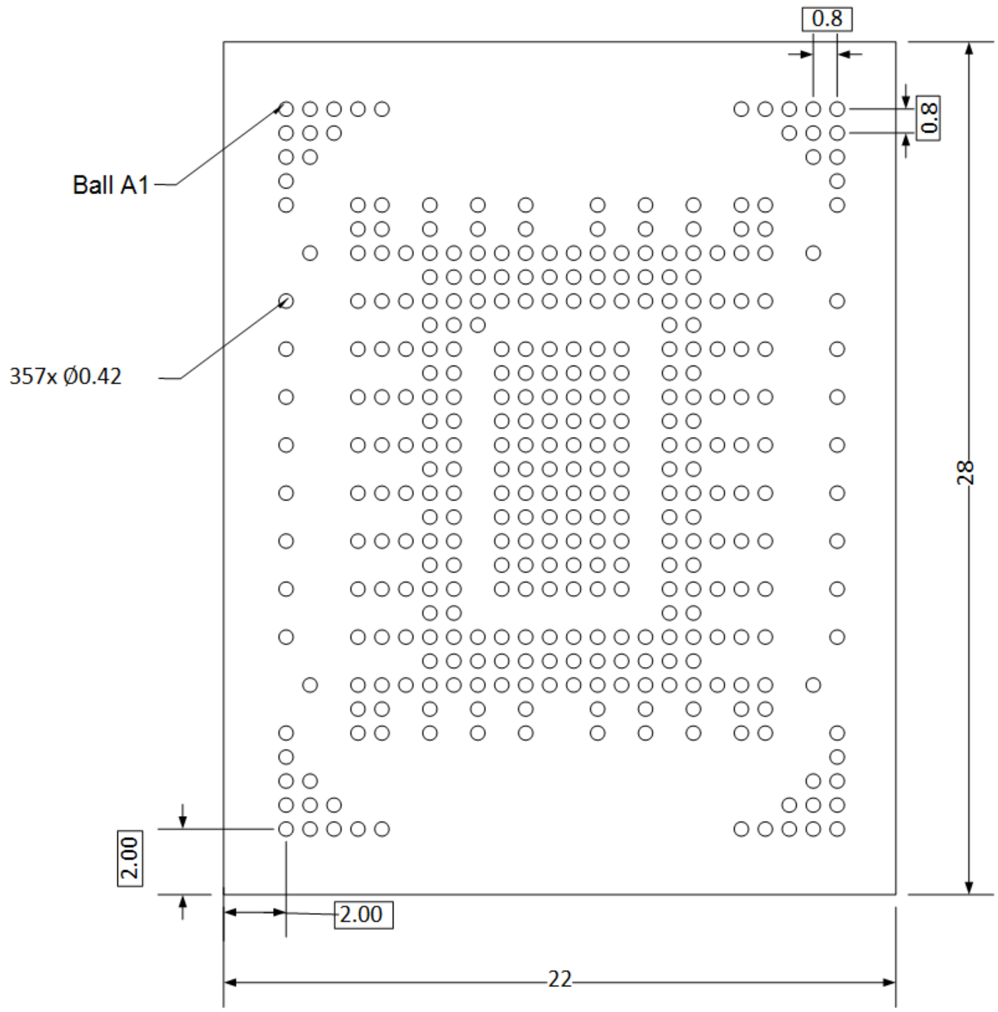


Figure 34. M.2 Type 2228-S5 Mechanical Outline Drawing Example



519

520 Figure 35. Recommended Land Pattern for M.2 Type 2228 BGA
521 (Top View)

2.3.6.4. Type 2828 Specification

Figure 36 shows an example of the M.2 Type 2828-S5 mechanical outline drawing and Figure 37 shows the recommended land pattern for Type 2828 package (dimensions shown in this figure are nominal).

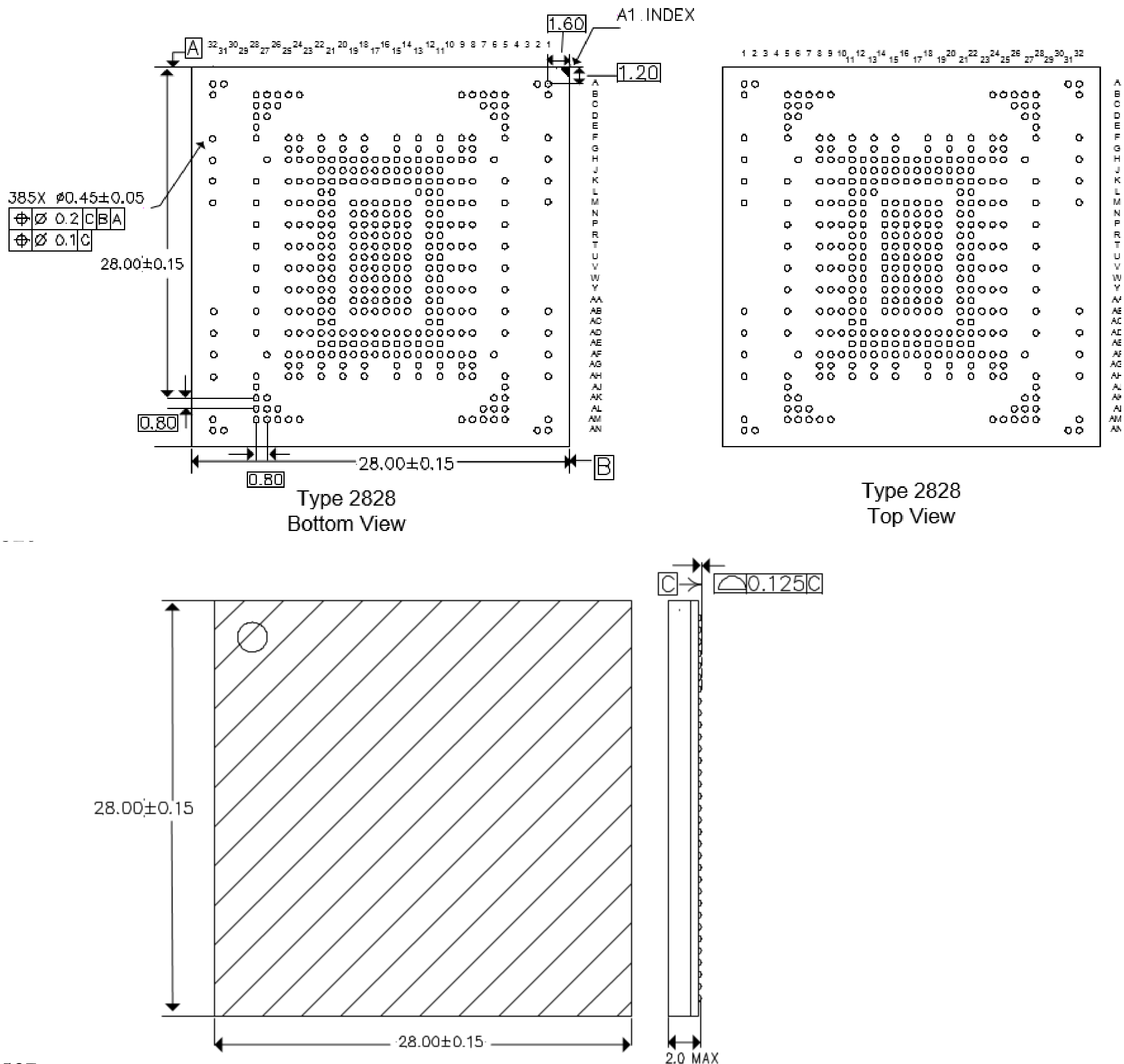


Figure 36. M.2 Type 2828-S5 Mechanical Outline Drawing Example

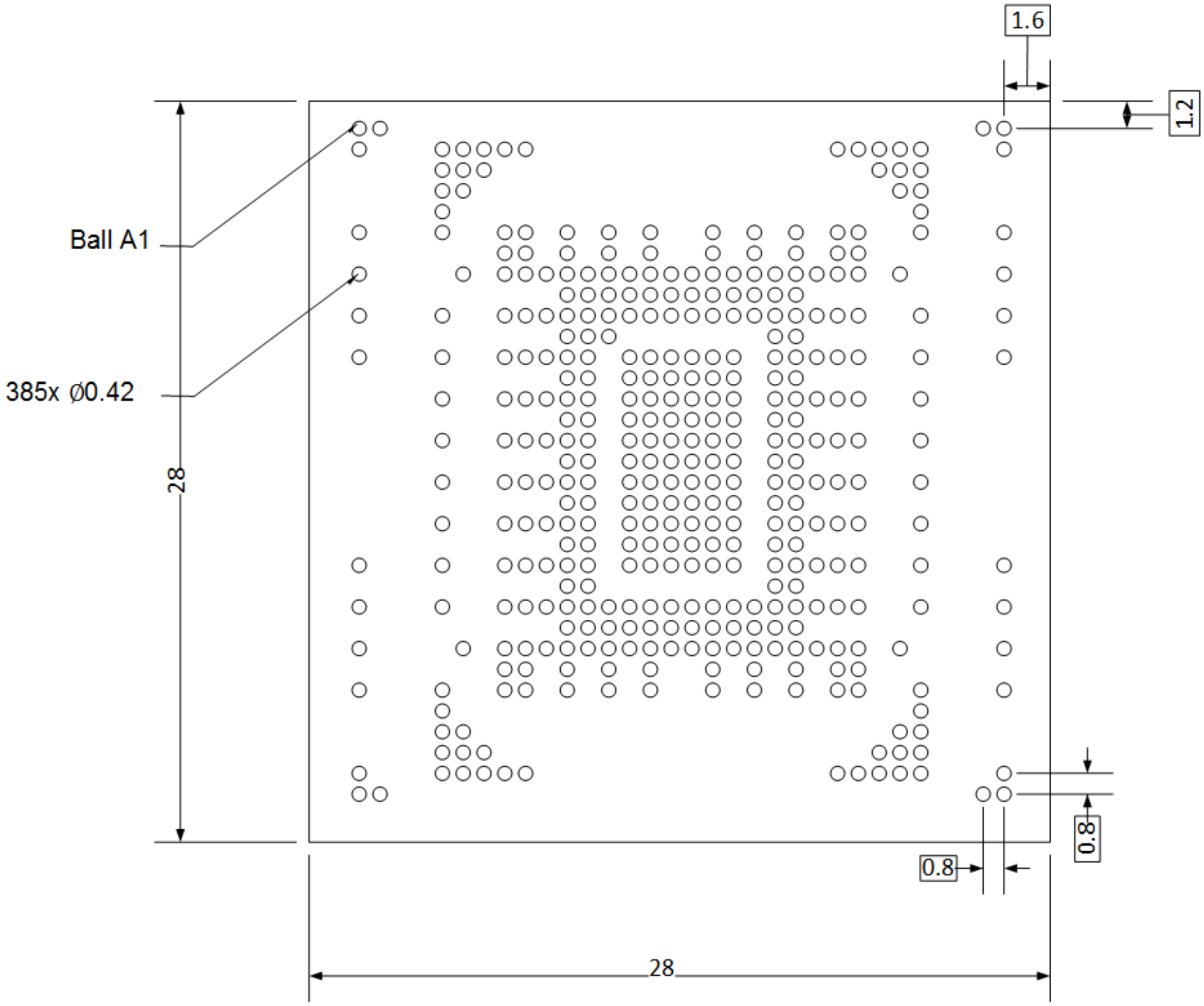


Figure 37. Recommended Land Pattern for M.2 Type 2828 BGA (Top View)

2.3.7. RF Connectors

The top end of the wireless Adapter board area is the preferred location for the RF connectors. However, other areas ~~can be~~are used in cases that this area is not enough at the expense of the component area (see Figure 38).

The standard 2x2 mm size RF receptacle connectors (see Figure 39) to be used in conjunction with the M.2 Adapters will accept two types of mating plugs that will meet a maximum Z-height of 1.45 mm (see Figure 40) utilizing a Ø 1.13 mm ~~coax cable~~(Diameter (Ø) = 1.13 mm) coax cable or a maximum Z-height of 1.2 mm using a Ø 0.81 mm coax cable (see Figure 41). Figure 42 shows the antenna connector designation scheme.

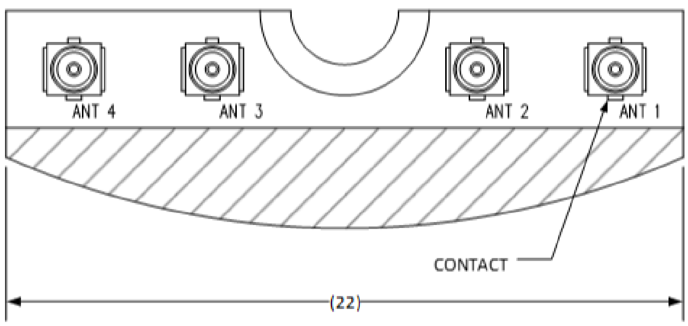


Figure 38. Board Type 2230 Antenna Connector Designation Scheme

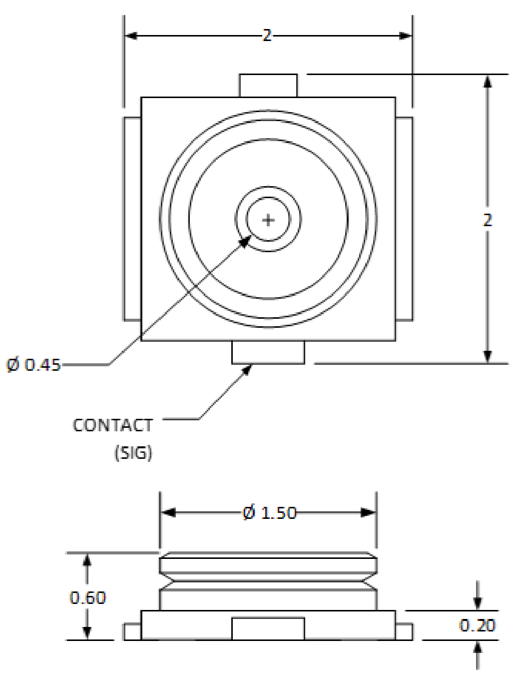


Figure 39. Generic 2x2 mm RF Receptacle Connector Diagram

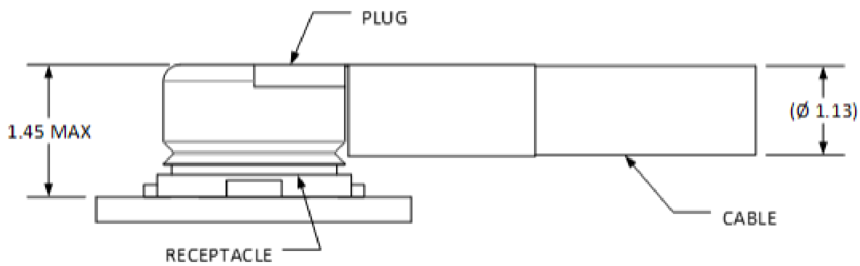


Figure 40. Mated Plug for Ø 1.13 mm Coax Cable

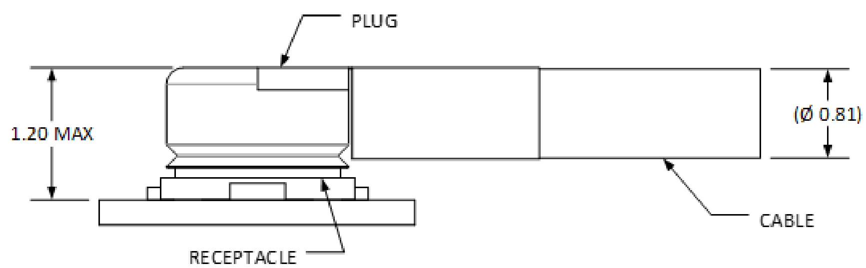


Figure 41. Mated Plug for Ø 0.81 mm Coax Cable

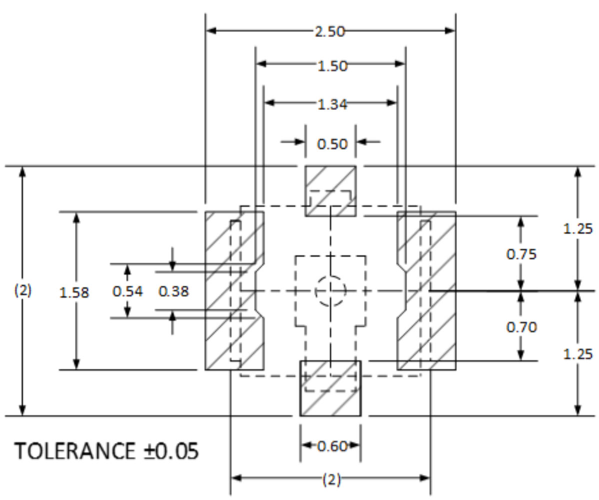


Figure 42. Antenna Connector PCB Recommended Land Pattern

Note: An optional Non-Plated Through Hole ~~may~~ is permitted ~~be placed~~ at the center of the land pattern for improved performance, enforcement of a trace Keep Out Zone and/or mechanical alignment. Example shown in Figure 28.

The minimum requirements for the RF Connector are listed in Table 5 ~~through~~ to Table 8.

- Table 5. RF Connector Physical Characteristics
- Table 6. RF Connector Mechanical Requirements
- Table 7. RF Connector Electrical Requirements
- Table 8. RF Connector Environmental Requirements

Table 5. RF Connector Physical Characteristics

Characteristic	Description
Receptacle Physical Outline	2 mm x 2 mm x 0.60 mm
Receptacle OD	1.5 mm
Housing Material	High Temperature Plastic
Flammability	UL 94-V0
Contact Material	Copper Alloy/Gold Plating
Ground Contact Material	Copper Alloy/Gold Plating

Table 6. RF Connector Mechanical Requirements

Description	Standard Requirement	Improved Requirement
Mating force	30 N Maximum	
Un-mating force	5 N Initial, 3 N Minimum after 30 cycles, 20 N Maximum	
Cable Retention at 0 Degree Pull (Parallel to PCB)	5 N Minimum	20 N Minimum (Ø 1.13 mm wire) 10 N Minimum (Ø 0.81 mm wire)
Cable Retention at 30 Degree Pull (PCB to Cable Angle)	Not Recommended	10 N Minimum
Durability (# of mating cycles)	30 cycles (Contact Resistance = -20 mΩ)	
Receptacle Shearing Strength	20 N Minimum	
Vibration	No momentary disconnections of 1 µs Minimum	

Table 7. RF Connector Electrical Requirements

Description	Requirements	Notes
Voltage Rating	60 V AC	
Current Rating	1.0 A Maximum	
Impedance	50 Ω	
Receptacle VSWR- 100 MHz ≤ f < ~~to about ~~~3 GHz~~(1)~~	1.3 Maximum	1
Receptacle VSWR- 3 GHz ≤ f < ~~to ~~~6 GHz~~(1)~~	1.45 Maximum	1
Optional Enhanced Frequency Receptacle VSWR- 3 GHz ≤ f < ~~to ~~~12 GHz~~(1,2)~~	2.0 Maximum	1, 2
Contact Resistance	Inner: 20 mΩ Maximum	
	Outer: 20 mΩ Maximum	
	Initial: 20 mΩ Maximum	
Dielectric Withstanding Voltage	200 V AC for one minute	
Insulation Resistance	500 mΩ for one minute at 100 V DC	

Note: ~~(1)~~1~~-~~. The VSWR of the receptacle is measured differently than the VSWR of the mating plug (see Section 6.4~~6.4~~).

~~(2)~~2~~-~~. The optional Enhanced frequency performance to 12 GHz to be provided upon specific request.

Table 8. RF Connector Environmental Requirements

Description	Requirement
Operating Temperature Range	-40 ˚C to +85 ˚C
Humidity	90%
Soldering Heat Resistance	Lead Free Reflow up to 260 ˚C peak for 10 s
RoHs Compliant/Halogen Free	Must be compliant

2.3.7.1. Socket 1 and 2 RF Connector Pinout

The RF Connector area will allow two (2), three (3), four (4), or six (6) RF connectors to be placed as a function of the board Type:

- Type 22xx ~~can~~ supports up to four RF Connectors
- Type 1630 ~~can~~ supports up to two RF Connectors
- Type 30xx ~~can~~ supports up to six RF Connectors
- Type 1216 ~~can~~ supports up to three RF Connectors

To remain consistent with the h~~H~~ost interface ~~I/F~~ pin order, the RF connectors are labeled ANT0, ANT1, ANT2, ANT3, ANT4, and ANT5 from right to left. The recommended antenna function allocation is given in Table 9~~Table 9~~.

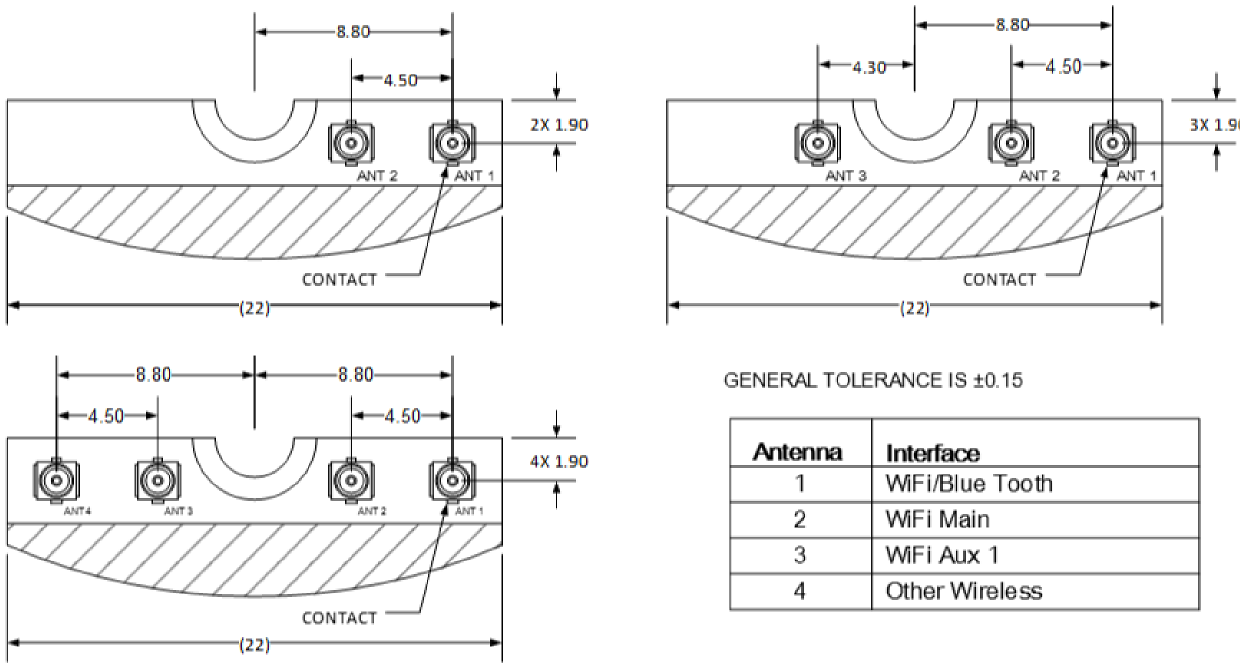
Table 9. Recommended Antenna Function Allocation Table

Type	ANT5	ANT4	ANT3	ANT2	ANT1	ANT0
Socket 1 WiFi+BT (Type 1630)	N/A	N/A	N/A	WiFi1	WiFi2+BT	N/A
Socket 1 WiFi+BT+Other (Type 2230, 3026, 3030, 2226)	N/A	Other Comm (when applicable)	WiFi3 (when applicable)	WiFi1	WiFi2+BT	N/A
Socket 2 (Key B) WWAN+GNSS (Type 2242, 3042)	N/A	VENDOR DEFINED	VENDOR DEFINED	VENDOR DEFINED	VENDOR DEFINED	N/A
Socket 2 (Key C) WWAN+GNSS (Type 2242, 3042)	VENDOR DEFINED	WWAN Main	VENDOR DEFINED	GNSS (Dedicated)	WWAN AUX and GNSS (when shared)	VENDOR DEFINED
Type 1216	N/A	N/A	VENDOR DEFINED	VENDOR DEFINED	VENDOR DEFINED	N/A

Note: Actual RF connector functions to be defined by vendor←→customer if not using the recommended allocations in this table.
ANT0 and ANT5 are an expansion of the basic four antenna connections (ANT1-ANT4) when the board is 30 mm wide.

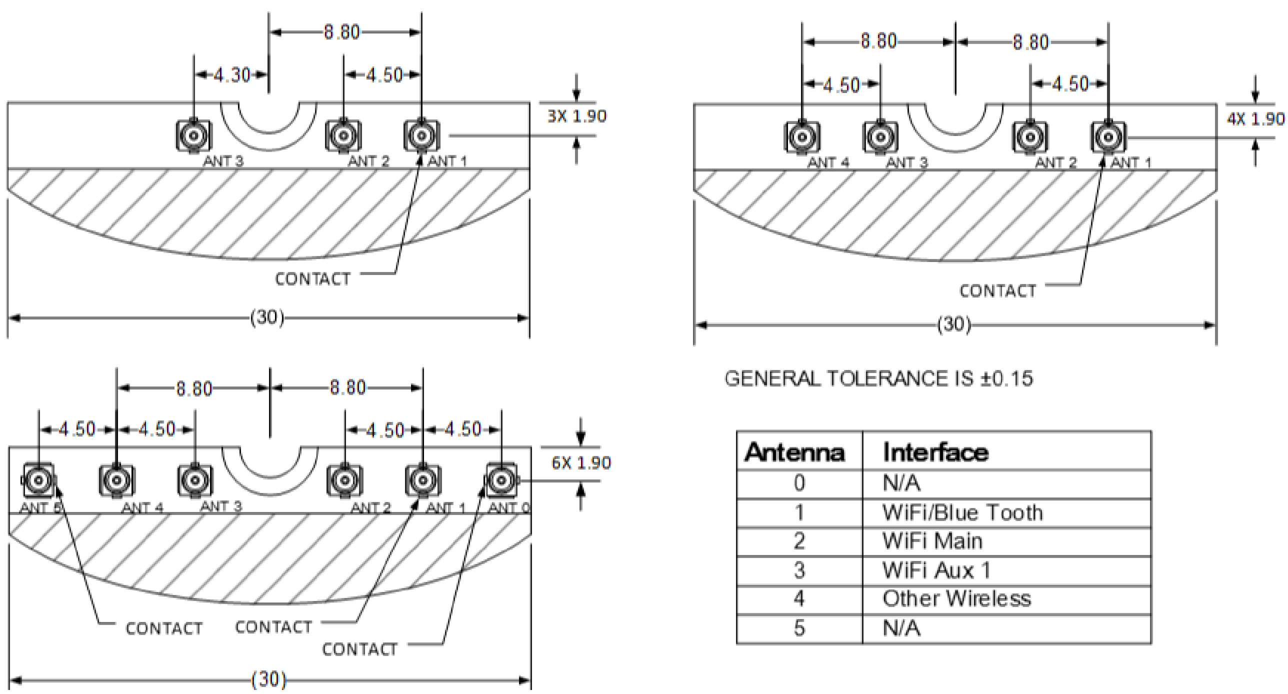
The recommended Wi-Fi antenna port assignment implies that the main Wi-Fi antenna port (~~for example~~e.g.~~;~~, Wi-Fi 1x1) would use ANT2 and listed as WiFi1. When Wi-Fi expands to a 2x2 configuration, it should share the antenna port with the BT using ANT1. This is listed as WiFi2+BT. In extended Wi-Fi 3x3 solutions, the third antenna port used is ANT3 and this is listed as WiFi3. Other Comms should use ANT4 when more complex wireless Combo solutions are implemented.

Figure 43 and Figure 44 show Socket 1 Type 2230 and 3030 RF connector assignment recommendations.



Antenna	Interface
1	WiFi/Blue Tooth
2	WiFi Main
3	WiFi Aux 1
4	Other Wireless

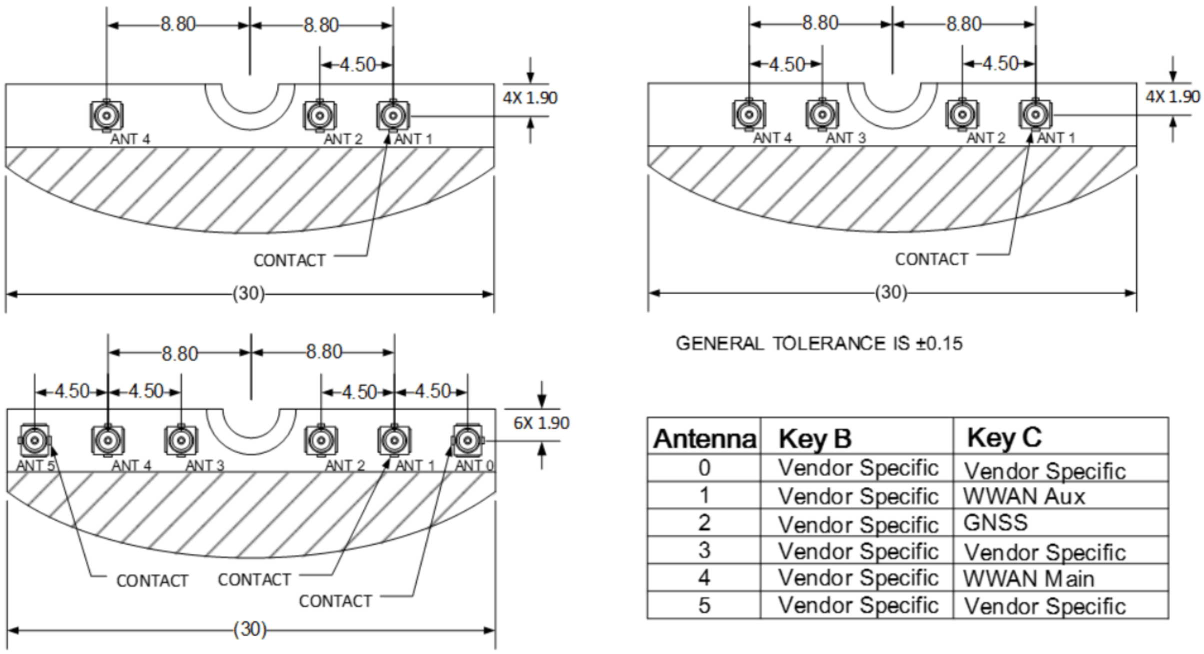
Figure 43. Socket 1 Type 2230 RF Connector Assignment Recommendation



Antenna	Interface
0	N/A
1	WiFi/Blue Tooth
2	WiFi Main
3	WiFi Aux 1
4	Other Wireless
5	N/A

Figure 44. Socket 1 Type 3030 RF Connector Assignment Recommendation

Socket 2 Key B Type 2242 and Type 3042 RF connector assignment recommendations are vendor-specific. The Socket 2 Key C Type 2242 and Type 3042 RF connector assignment recommendation are listed in Table 9 and ~~can be~~are seen in Figure 45.



Antenna	Key B	Key C
0	Vendor Specific	Vendor Specific
1	Vendor Specific	WWAN Aux
2	Vendor Specific	GNSS
3	Vendor Specific	Vendor Specific
4	Vendor Specific	WWAN Main
5	Vendor Specific	Vendor Specific

Figure 45. Socket 2 Type 2242/3042 RF Connector Assignment Recommendation

2.4. System Connector Specifications

The card interconnect is based on a 75 position Edge Card connector. The 75 position connector is intended to be keyed so as to distinguish between families of ~~Host~~ host ~~Interfaces~~ interfaces and the various Sockets used in NB/very thin ~~platforms~~ Platforms and Tablet ~~platforms~~Platforms. This specification document makes provision for the following three Socket families:

- Connectivity Socket 1
- WWAN/SSD/Other Socket 2
- SSD Drive Socket 3

In order to accommodate various product Z-height limitations, there will be generic types of Edge Connectors in multiple height variants designated below:

- M1.8 – Mid-mount (1.80 mm Max height (Ht.)) – For very low profile ~~platforms~~Platforms
- H2.3 – Top-side – Single-sided (2.25 mm Max Ht.) Connector
- H2.5 – Top-side – Single-sided (2.45 mm Max Ht.) Connector
- H2.8 – Top-side – Double-sided (2.75 mm Max Ht.) Connector
- H3.2 – Top-side – Double-sided (3.20 mm Max Ht.) Connector
- H4.2 – Top-side – Double-sided (4.20 mm Max Ht.) Connector

This list of connector options is not exclusive; other connector designs are allowed per market needs, however they must meet normative mechanical and electrical requirements contained within this document.

> ~~**Note:** This list of connector options is not exclusive; other connector designs are allowable per market needs, however they must meet normative mechanical and electrical requirements contained within this document.~~

Table 10~~Table 10~~ lists the Adapter heights supported by the different connector types.

Table 10. Connector/Adapter Height Supported Matrix

	Description	Component Height Descriptors									
		S1	S2	S3	S4	S5	D1	D2	D3	D4	D5
M1.8	Mid-mount Connector	✓	✓	✓	✓	✓	✓	✓	✓ (see Note)	✓	✓
H2.3	Single-sided (2.25 Max Ht.) Connector	✓	✓	✓	✓	✓					
H2.5	Single-sided (2.45 Max Ht.) Connector	✓	✓	✓	✓	✓					
H2.8	Double-sided (2.75 Max Ht.) Connector	✓	✓	✓	✓	✓				✓	

H3.2	Double-sided (3.2 Max Ht.) Connector	✓	✓	✓	✓	✓	✓	✓	✓	✓	
H4.2	Double-sided (4.2 Max Ht.)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Note: * System clearance will have to be evaluated.											

The Hx naming convention along with the mechanical Key letter enables easy recognition of the required connector through simple nomenclature; as shown in the following example:

M.2 Connector H2.3-E-Opt1

- **H2.3** designates the connector height; in this case the height supports a Single-sided solution (2.25 mm Max Ht.).
- **E** designates Key E.
- **Opt1** designates the durability level, the minimum number of insertion/extraction cycles, in this case a minimum of 25 (see the Durability line item in Table 12).

This Hx descriptor also aligns with the coinciding Standoff descriptor described in the Section 2.5.

2.4.1. Connector Pin Count

The connector has 75 positions. However, eight positions are used for each connector key so the pin count is 67 pins.

2.4.2. Contact Pitch

The contact pitch is 0.5 mm. The connector will have two rows of pins, top and bottom. The bottom row is staggered by 0.25 mm from the top row.

2.4.3. System Connector Parametric Specifications

Table 11, Table 12, and Table 13 specify the requirements for physical, environmental, and electrical performance for the M.2 connector.

Table 11. Connector Physical Requirements

Description	Requirement
Connector Housing	UL rated 94-V-0 Must be compatible with lead-free soldering process
Contact: Receptacle	Copper alloy with Gold Plating sufficient to meet all mechanical and environmental requirements
Contact Finish: Receptacle	Must be compatible with lead-free soldering process

Table 12. Connector Environmental Requirements

Test Conditions	Specification
Durability	EIA-364-9:~~;~~ • Option 1 - 25 cycles~~,~~ • Option 2 - 60 cycles~~.~~ Upon completion of cycles the sample must meet all visual and electrical performance requirements.
Insertion Force	Insertion Force-25 N (2.04 KgF, ~~-~~1 Newton = 1 Kg. ~~*~~m/s^2) maximum EIA-364-13, Method A
Shock	• 250 G (Notebook) and 285 G (Tablet) • At 2 ms half sine • On all six (6) axis
Vibration	EIA-364-1000 Test group 3, EIA-364-28
Operating Temperature	-40~~°C~~ °C to 80~~°C~~ °C
Environmental Test Methodology	EIA-364-1000 Test Group 1, 2, 3, and 4
Useful Field Life	Three years

Table 13. Connector Electrical Requirements

Description	Requirement
Low Level Contact Resistance	EIA-364-23 • 55 mΩ maximum (initial) per contact • 20 mΩ maximum change allowed
Insulation Resistance	EIA-364-21 • >5 x 108 Ω @ 500 V DC
Dielectric Withstanding Voltage	EIA-364-20 • >300 V AC (RMS) @ Sea Level
Current Rating	• 0.5 A/Power Contact (continuous) • The temperature rise above ambient ~~shall~~ must not exceed 30 °C. • The ambient condition is still air at 25 °C. • EIA-364-70 Method 2
Voltage Rating	50 V AC per Contact

2.4.4. Additional Environmental Requirements

The connector must meet RoHS (no exceptions) and Low Halogen compliance.

2.4.5. Card Insertion

- Angled insertion is allowable and preferred; intent is to minimize the insertion/extraction force. The minimum of angle of insertion is 5° (see Figure 46)
- Minimum two step insertion is desirable; intent is to minimize the insertion/extraction force.

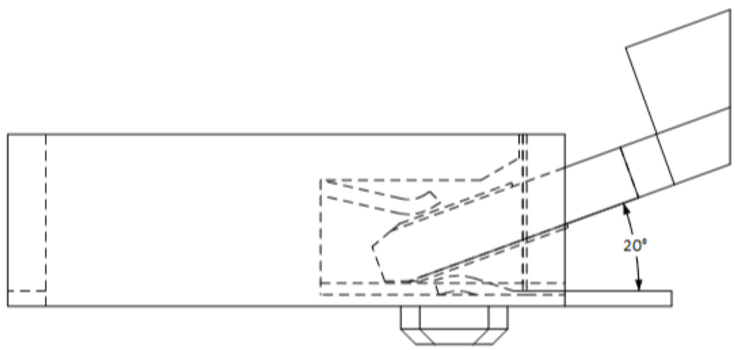


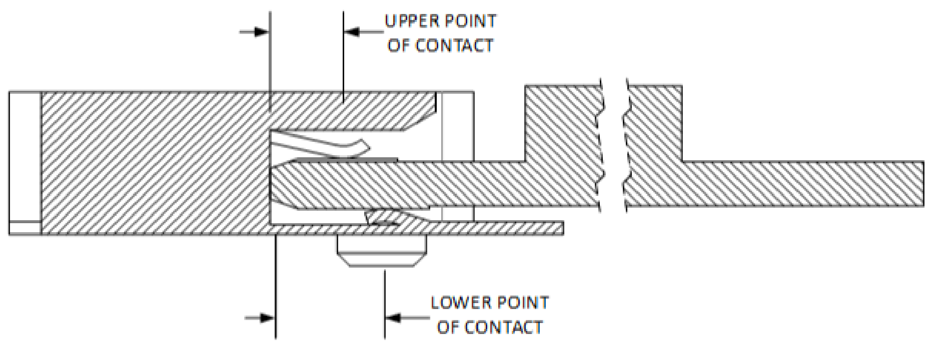
Figure 46. Angle of Insertion

2.4.6. Point of Contact Guideline

The signal integrity and mechanical requirements yield a starting point for the point of contact to Add-in Card Gold Finger relationship. The range for the upper point of contact measured from the seating plane should be between 0.8 mm to 1.3 mm and the range for the lower point of contact should be between 0.9 mm to 2.2 mm. (see Figure 47~~, Point of Contact~~).

Notwithstanding the aforementioned, the actual mechanical relationship between connector and Add-in Card within a system is controlled by the ~~platform~~ Platform implementer. ~~Therefore~~Therefore, ~~platform~~ Platform implementers should pay attention to all elements of positioning connector and Add-in Card to assure a proper mated condition.

Note: The angle of insertion is a key consideration for determining the point of contact; see Figure 47. Objective is to minimize insertion/removal forces while meeting signal integrity requirements.



Note: Connector design and contact shape are generic and infers no design intent beyond the dimensioned contact point.

Figure 47. Point of Contact

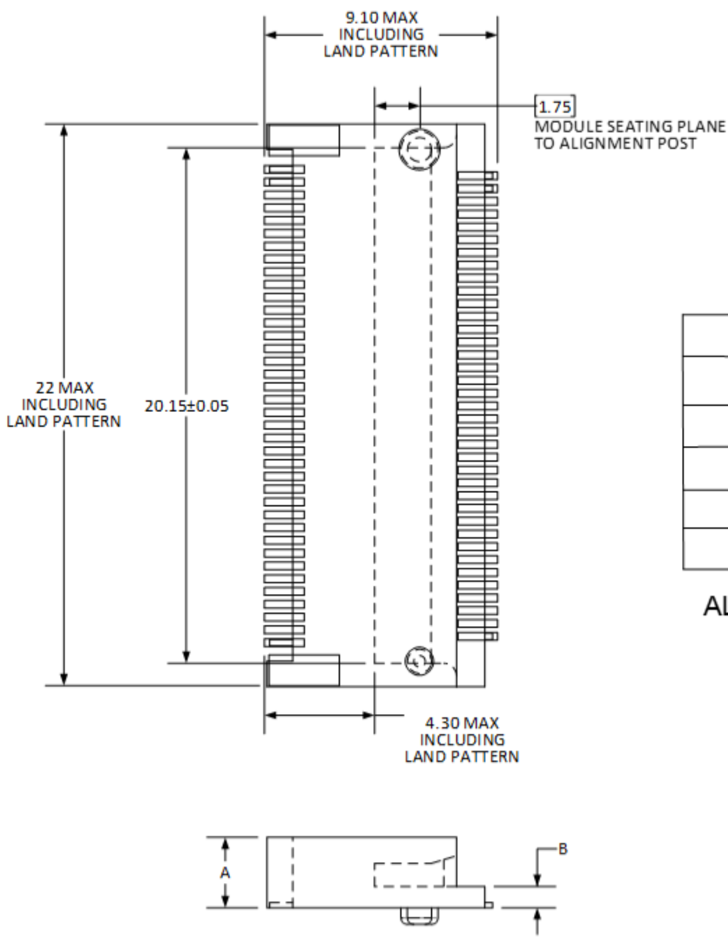
2.4.7. Top-side Connection

2.4.7.1. Top-side Connector Physical Dimensions

The top-side scheme has two connectors that share a common footprint but have a different stack-up requirement (see S~~s~~ection 2.4.7.3~~, Top-side Connection Stack-up,~~ for more detail)

- Length—22 mm maximum including land pattern
- Width—9.1 mm maximum including land pattern

Figure 48 shows the top-side connector dimensions.



Height	A (MAX)	B (MAX)
H2.3	2.25	0.41
H2.5	2.45	0.61
H2.8	2.75	0.89
H3.2	3.20	1.54
H4.2	4.20	2.54

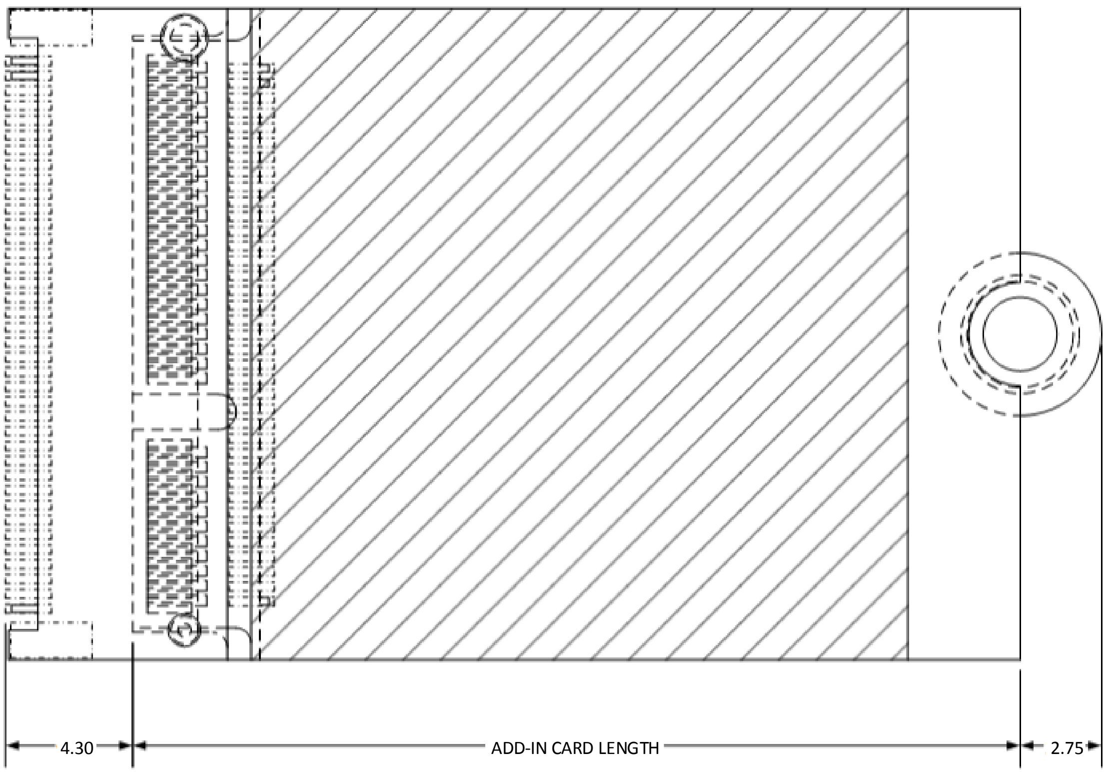
ALL DIMENSIONS mm

Figure 48. Top-side Connector Dimensions

2.4.7.2. Top-side Connection Total System Length

The maximum total solution is constrained to the Add-in Card length plus the following increases:

- The additional increase in length is 7.05 mm maximum for top-side connector to the Add-in Card length (see Figure 49).
  - The retention screw adds 2.75 mm maximum.
  - The maximum extension, including land pattern beyond the Add-in Card leading edge is 4.3 mm.
- Add-in Card lengths are 30 mm, 42 mm, 60 mm, 80 mm, and 110 mm.



Note: The retention screw and stand-off are required for mechanical hold down and potential thermal path (see Ssection 2.5~~, Module Stand-off for an example~~).

Figure 49. Top Mounting System Length

2.4.7.3. Top-side Connection Stack-up

2.4.7.3.1. Single-sided Add-in Card (Using H2.3 Connector)

Total solution above the main board (MB) varies based on the maximum component height on the Add-in Card. Figure 50, Figure 51, and Figure 52 show the profiles based on three single-sided maximum component heights; 1.2 mm, 1.35 mm, and 1.5 mm. The maximum Root Sum Square (RSS) given is calculated from the top of the main board to the top of the Add-in Card.

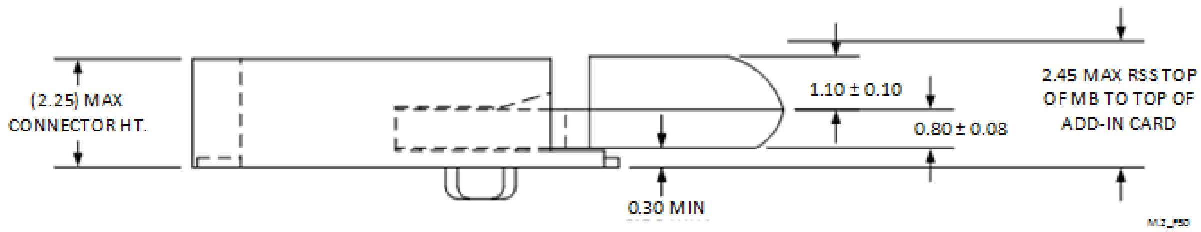


Figure 50. H2.3-S1 - Stack-up Top Mount Single-sided Add-in Card for 1.2 Maximum Component Height

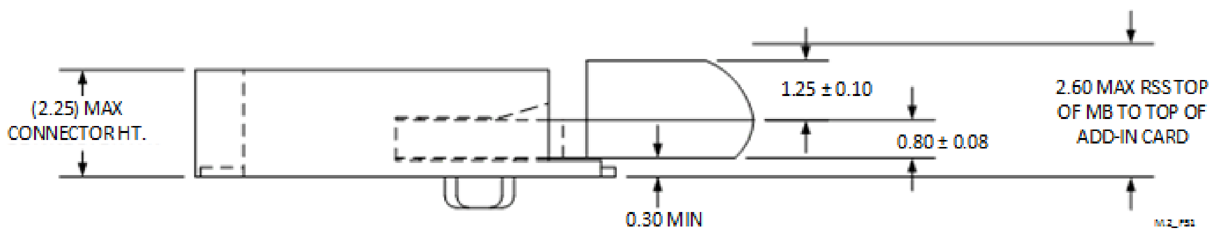


Figure 51. H2.3-S2 - Stack-up Top Mount Single-sided Add-in Card for 1.35 Maximum Component Height

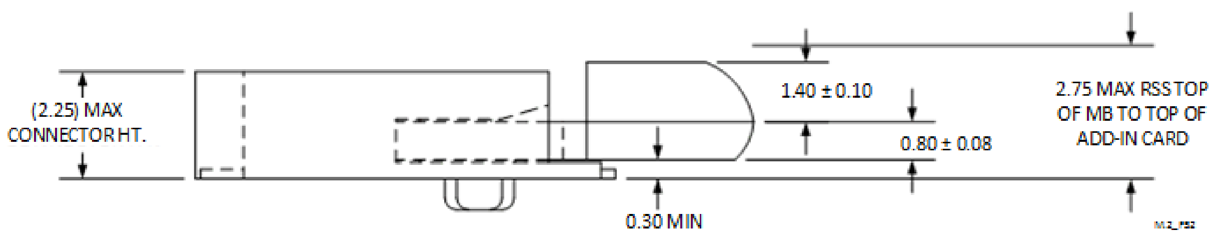


Figure 52. H2.3-S3 - Stack-up Top Mount Single-sided Add-in Card for 1.50 Maximum Component Height

2.4.7.3.2. Single-sided Add-in Card (Using H2.5 Connector)

Total solution above the main board varies based on the maximum component height on the Add-in Card. Figure 53, Figure 54, and Figure 55 show the profiles based on three single-sided maximum component heights; 1.2 mm, 1.35 mm, and 1.5 mm. The maximum RSS given is calculated from the top of the main board to the top of the Add-in Card.

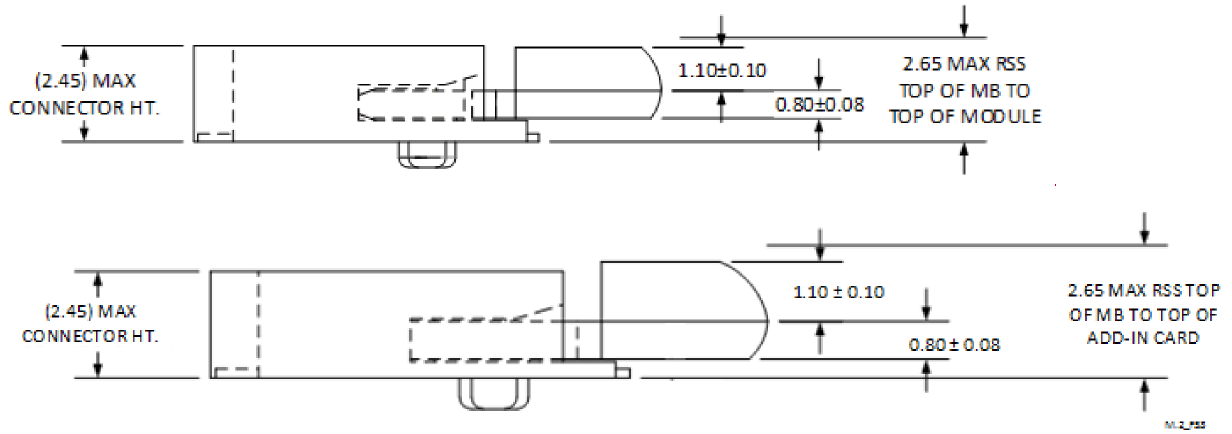


Figure 53. H2.5-S1 - Stack-up Top Mount Single-sided Add-in Card for 1.20 Maximum Top-side Component Height and with Higher Clearance above ~~Motherboard~~Motherboard

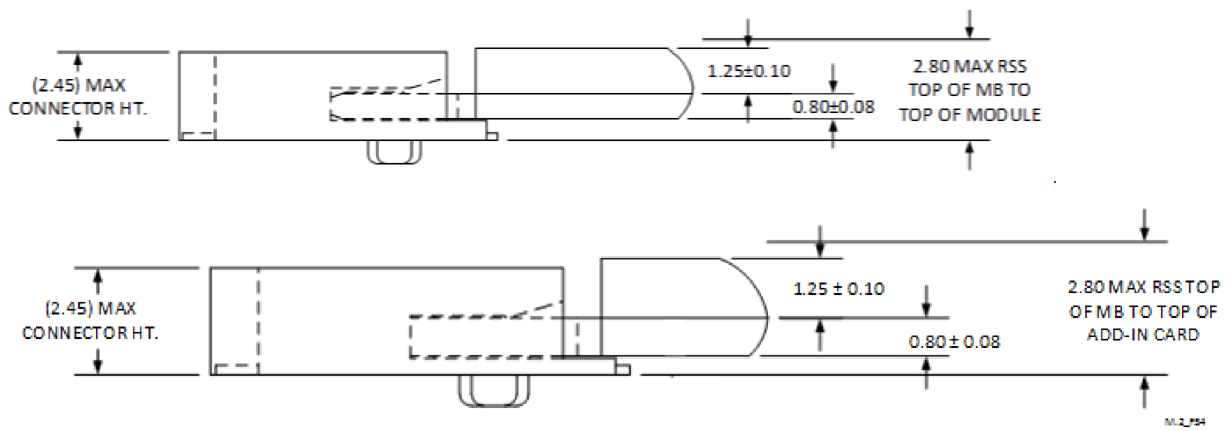


Figure 54. H2.5-S2 - Stack-up Top Mount Single-sided Add-in Card for 1.35 Maximum Top-side Component Height and with Higher Clearance above ~~Motherboard~~Motherboard

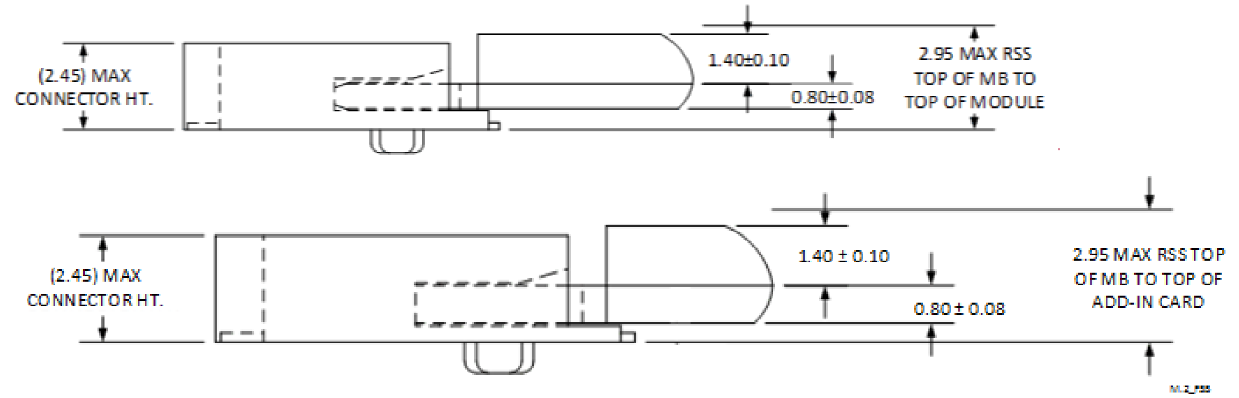


Figure 55. H2.5-S3 - Stack-up Top Mount Single-sided Add-in Card for 1.5 Maximum Top-side Component Height and with Higher Clearance above ~~Motherboard~~Motherboard

2.4.7.3.3. Double-sided Add-in Card (Using H2.8, H3.2 and H4.2 Connector)

Total solution above the main board varies based on the maximum component height on the Add-in Card. Figure 56, Figure 57, Figure 58, Figure 59, and Figure 60, show the profiles based on three top-side maximum component heights; 1.2 mm, 1.35 mm, and 1.5 mm. The bottom-side components maximum height is 1.50 mm, 1.35 mm, or 0.70 mm. The maximum RSS given is calculated from the top of the main board to the top of the Add-in Card.

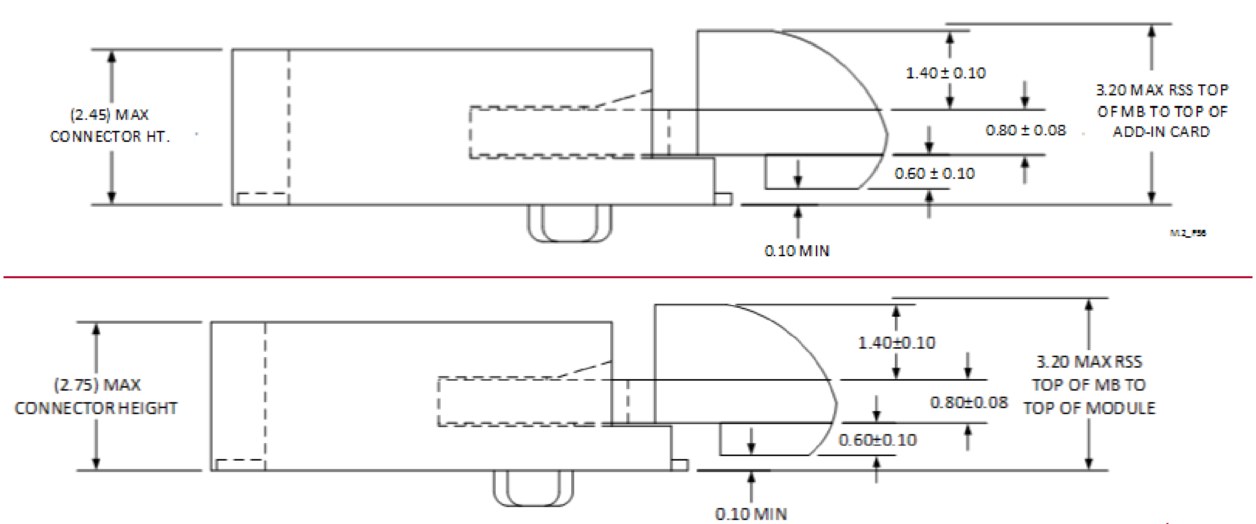


Figure 56. H2.8-D4 - Stack-up Top Mount Double-sided Add-in Card for 1.5 Maximum Top-side Component Height with 0.7 Maximum Bottom-side Component Height

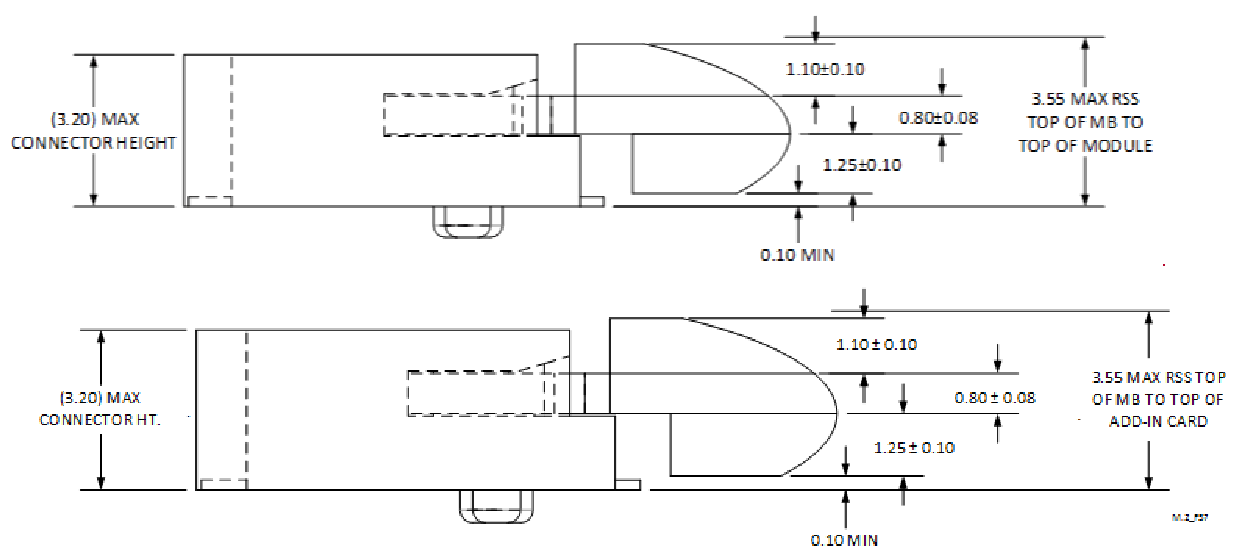


Figure 57. H3.2-D1 - Stack-up Top Mount Double-sided Add-in Card for 1.20 Maximum Top-side Component Height

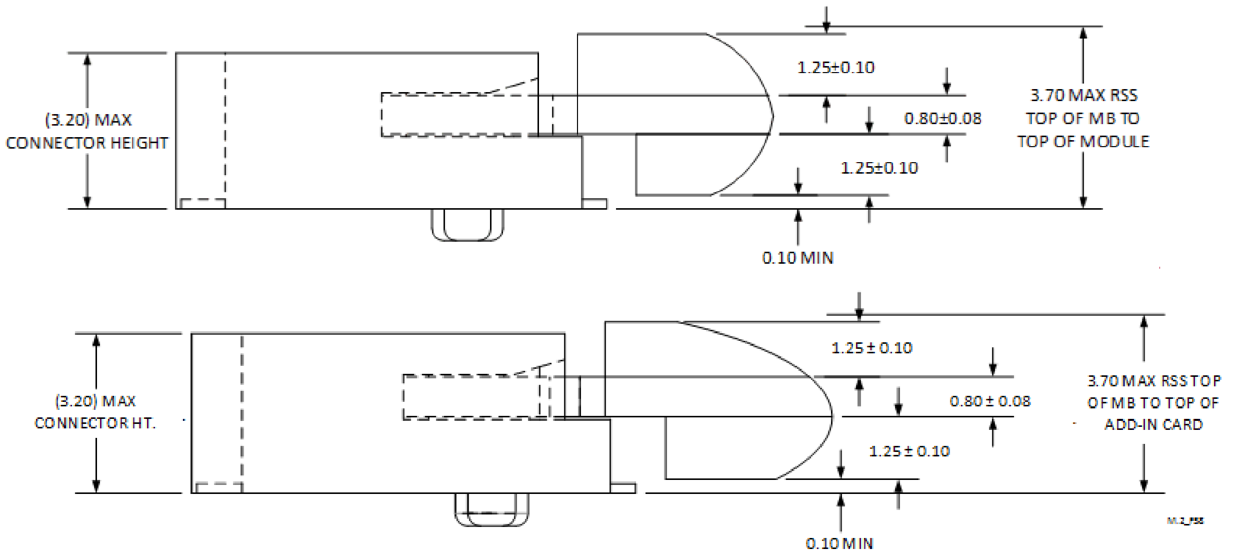


Figure 58. H3.2-D2 - Stack-up Top Mount Double-sided Add-in Card for 1.35 Maximum Top-side Component Height

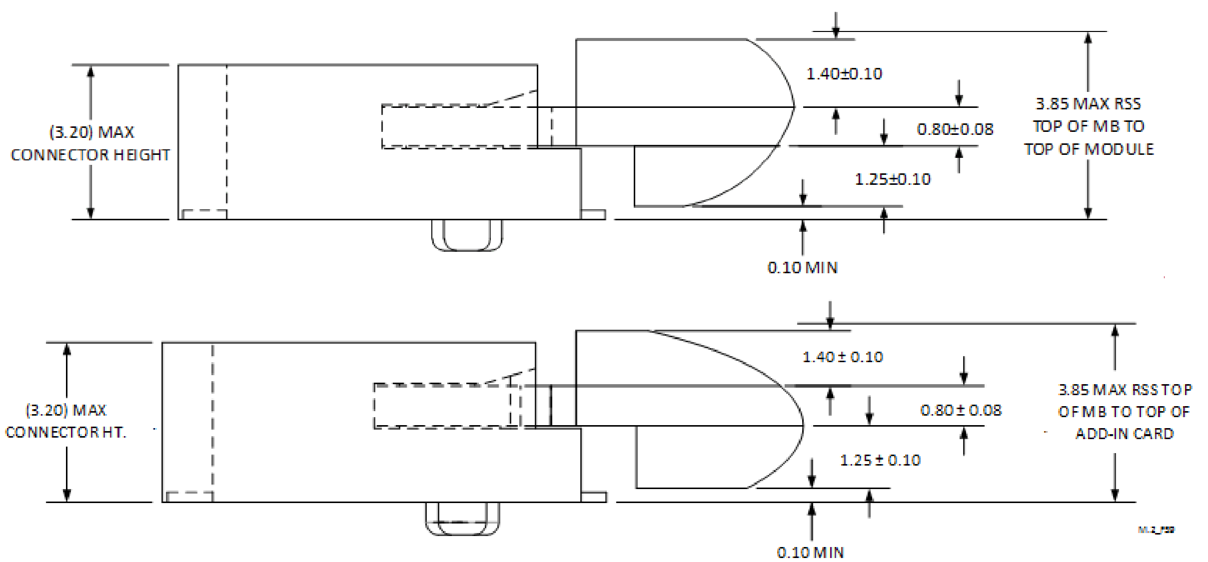


Figure 59. H3.2-D3 - Stack-up Top Mount Double-sided Add-in Card for 1.5 Maximum Top-side Component Height

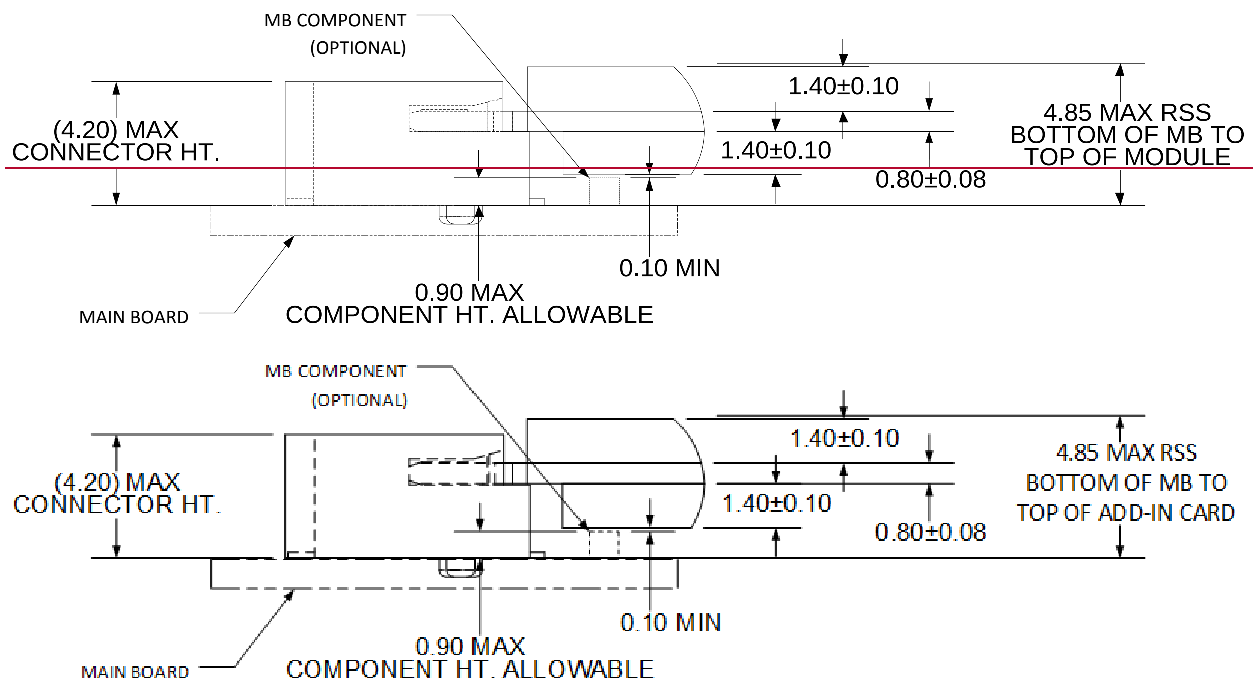


Figure 60. H4.2-D5 - Stack-up Top Mount Double-sided Add-in Card for 1.5 Maximum Top-side Component Height with 1.5 Maximum Bottom-side Component Height

2.4.7.4. Top-side Connector Layout Pattern

The layout footprint of the Top Mount ~~Host I/F Edge Card Slot~~ connector on the Platform side ~~Mother Board~~ is shown in Figure 61. The land pattern includes all 75 pads although only up to 67 pads will be routed out while eight (8) pads will be redundant as they are located where the Mechanical Key is located. Figure 61 shows the eight redundant pads of Key B as faded.

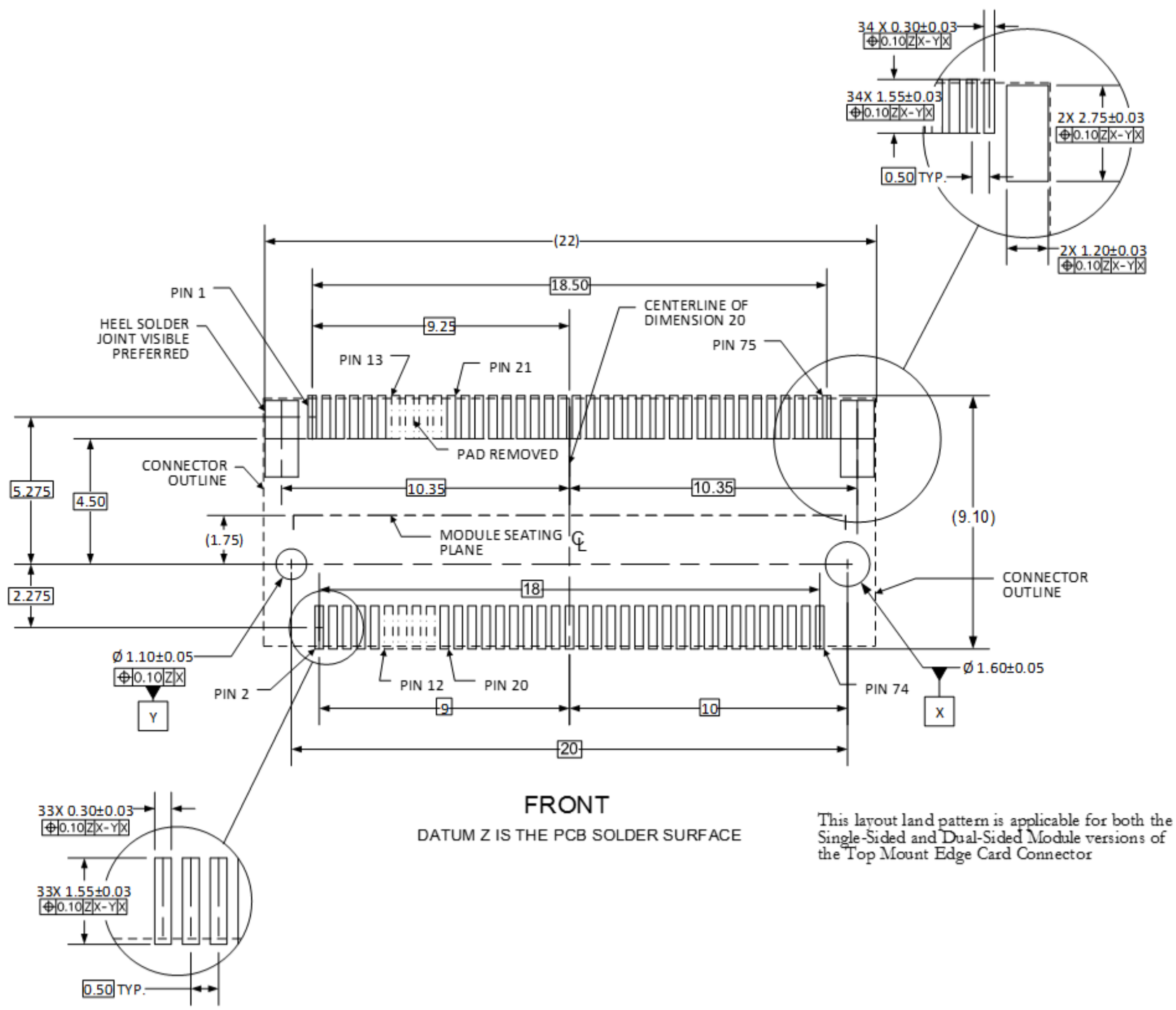


Figure 61. Example of Top Mount ~~Motherboard~~Motherboard Land Pattern—~~Diagram~~
~~-~~Key B Shown

2.4.8. Mid-mount Connection (Using M1.8 Connector)

2.4.8.1. Mid-mount Connector Physical Dimensions

- Length-24 mm maximum including land pattern (see Figure 62)
- Width-9.5 mm maximum including land pattern

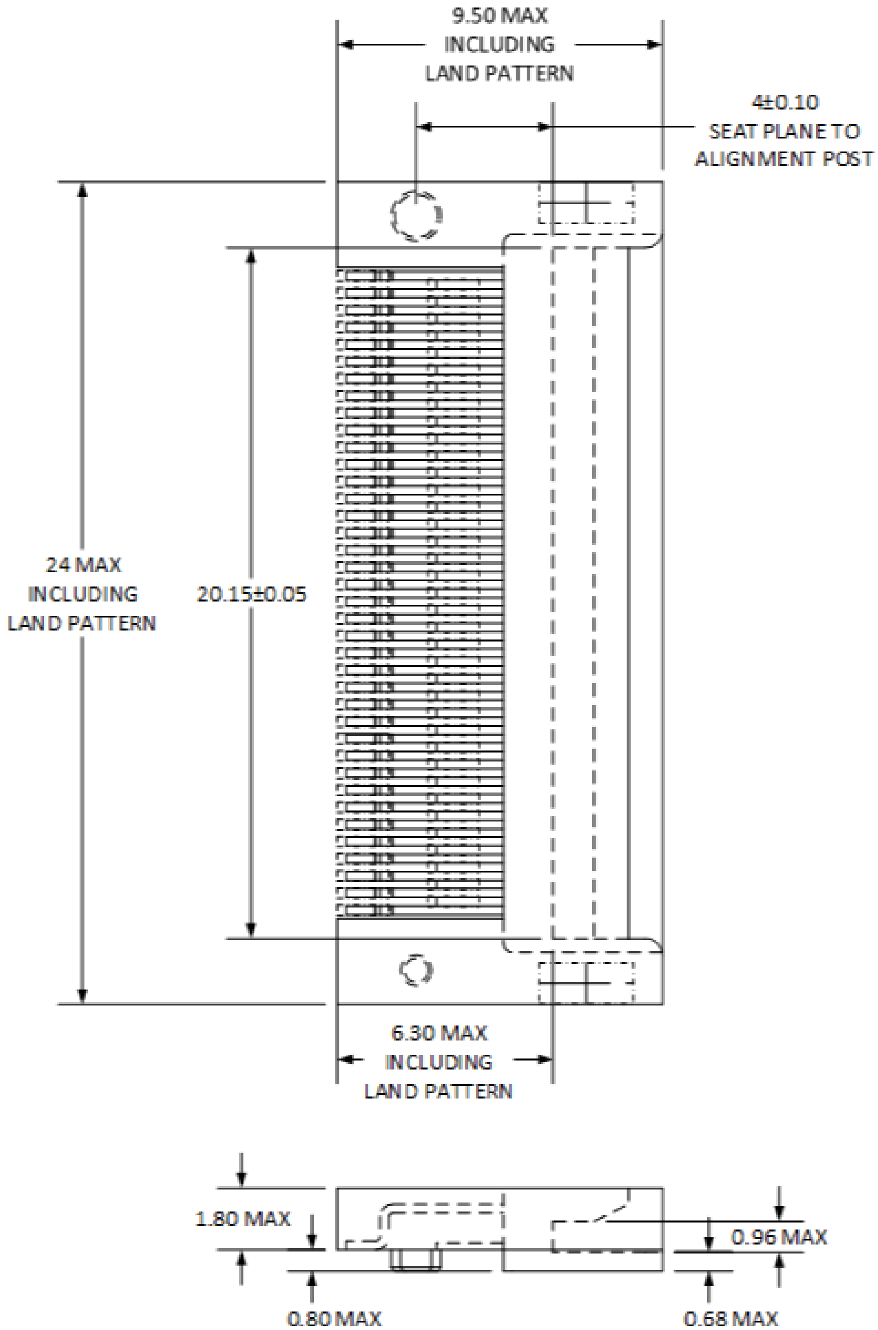


Figure 62. Mid-mount (In-line) Connector Dimensions

2.4.8.2. Mid-mount Connection Total System Length

The maximum total solution is constrained to ~~module~~ Add-in Card length plus the following increases (see Figure 63):

- The additional increase in length is 9.05 mm for top-side connector to the Add-in Card ~~module~~ length:~~.~~
  - The retention screw adds 2.75 mm maximum.
  - The maximum extension, including land pattern beyond the Add-in Card ~~module~~ leading edge is 6.3 mm.
- Add-in Card ~~Module~~ lengths are 30 mm, 42 mm, 60 mm, 80 mm, and 110 mm.

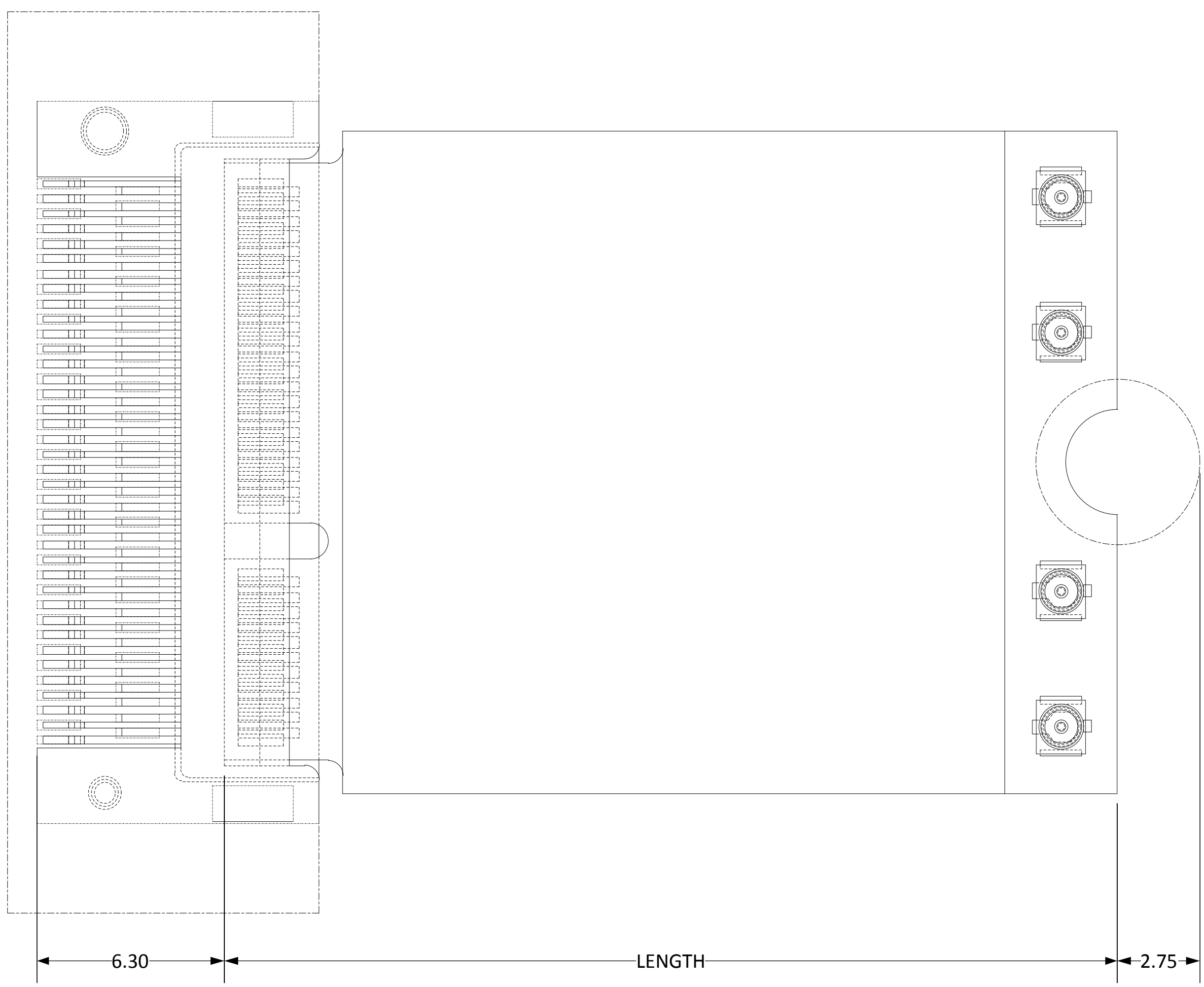


Figure 63. Mid-mount (In-line) System Length

2.4.8.3. Mid-mount Connection Stack-up

2.4.8.3.1. Single-sided Add-in Card ~~Module~~

Total solution above the main board varies based on the maximum component height on the Add-in Card ~~module~~. Figure 64, Figure 65, and Figure 66 show the profiles based on three single-sided maximum component heights; 1.2 mm, 1.35 mm, and 1.5 mm. The maximum RSS given is measured from the top of the main board to the top of the Add-in Card ~~module~~. Also given is the maximum RSS as calculated from the bottom of the main board to top of the Add-in Card ~~module~~.

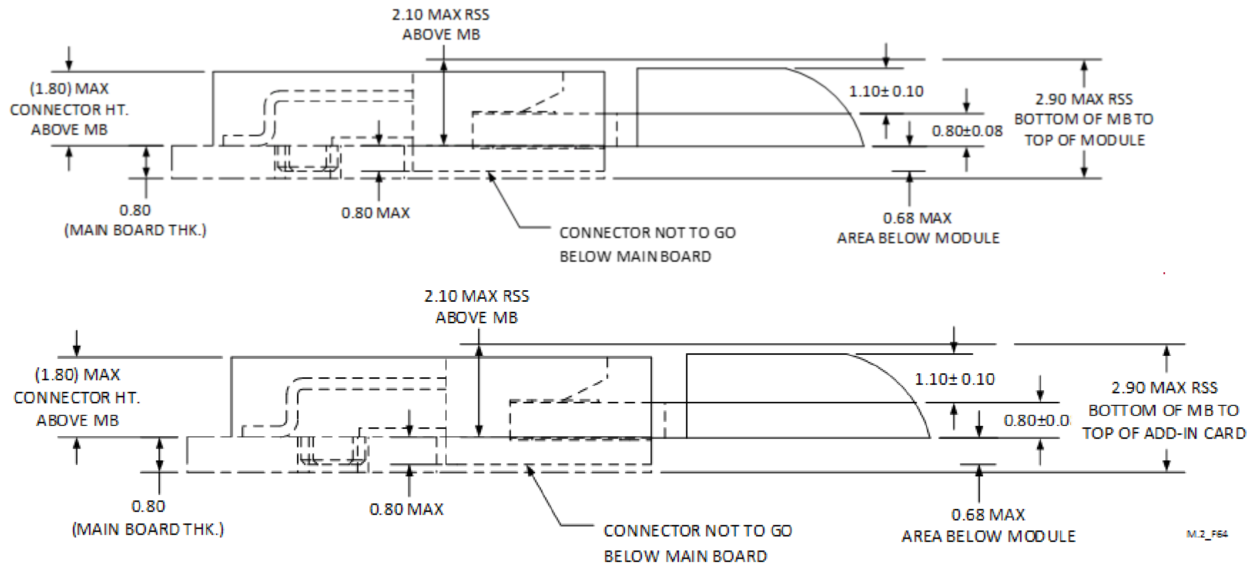


Figure 64. Stack-up Mid-mount (In-line) Single-sided (S1) ~~Module~~ Add-in Card for 1.2 Maximum Component Height

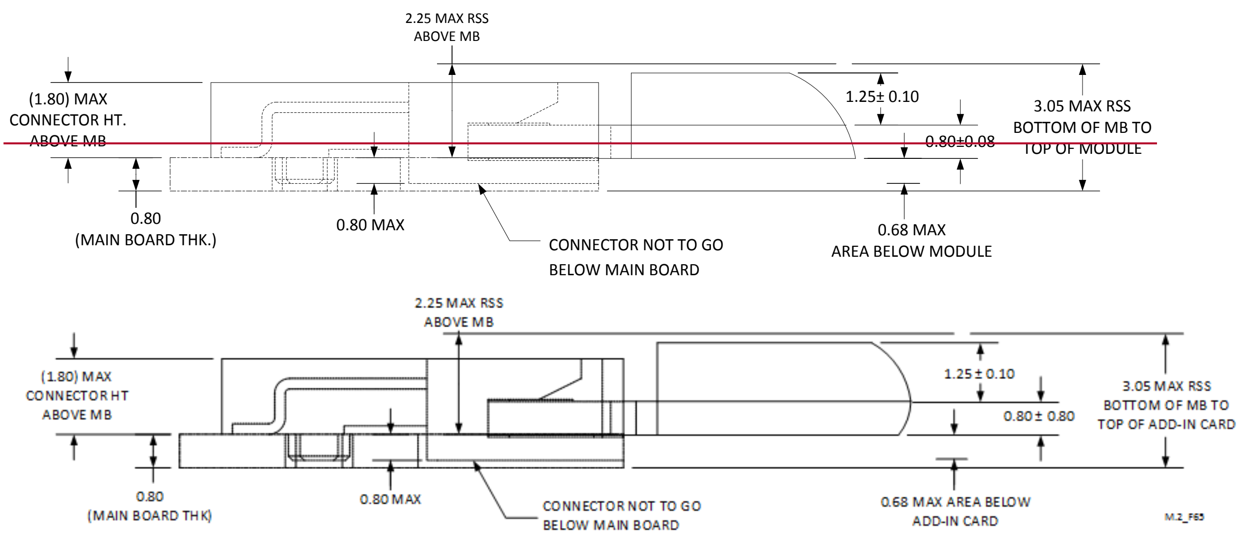
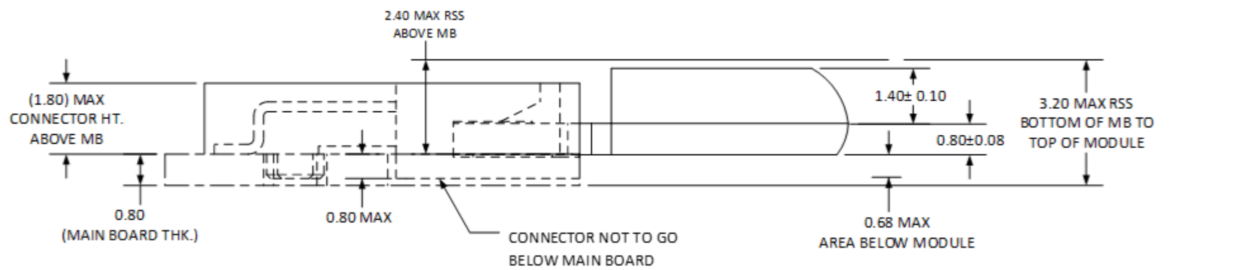


Figure 65. Stack-up Mid-mount (In-line) Single-sided (S2) Add-in Card ~~Module~~ for 1.35 Maximum Component Height



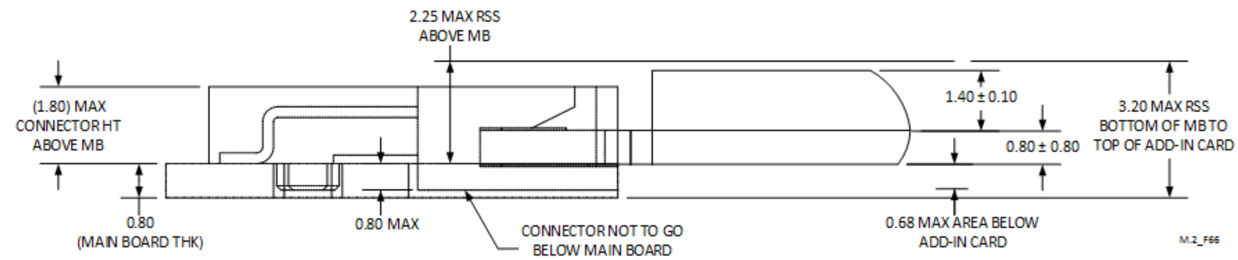


Figure 66. Stack-up Mid-mount (In-line) Single-sided (S3) Add-in Card ~~Module~~ for 1.5 Maximum Component Height

2.4.8.3.2. Double-sided ~~Module~~Add-in Card

Total solution above the main board varies based on the maximum component height on the ~~module~~Add-in Card. Figure 67 through Figure 71 show the profiles based on three top-side maximum component heights; 1.2 mm, 1.35 mm, and 1.5 mm. The bottom-side components maximum height is 1.5 mm, 1.35 mm, or 0.7 mm. The maximum RSS given is calculated from the top of the main board to the top of the Add-in Card~~module~~.

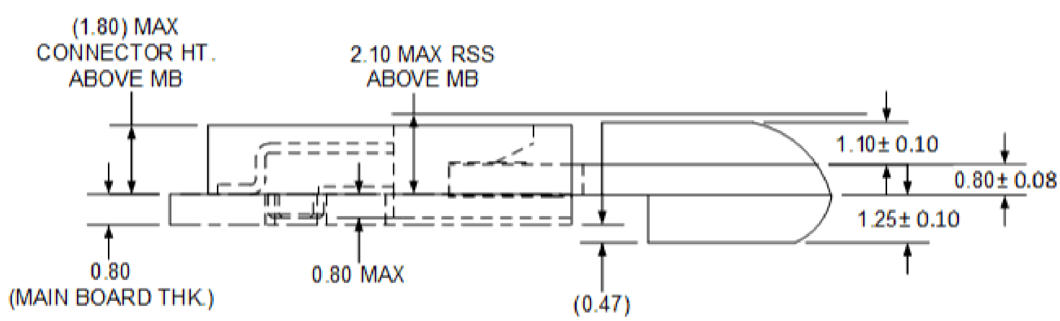


Figure 67. Stack-up Mid-mount (In-line) Double-sided (D1) Add-in Card ~~Module~~ for 1.2 Maximum Top-side Component Height

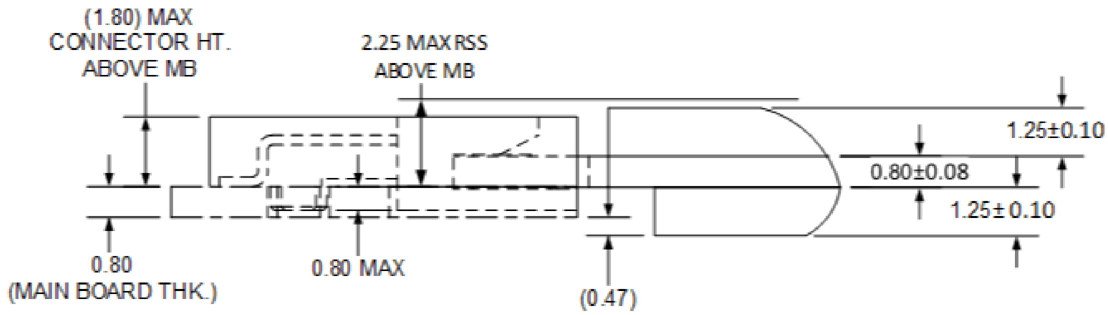


Figure 68. Stack-up Mid-mount (In-line) Double-sided (D2) Add-in Card ~~Module~~ for 1.35 Maximum Top-side Component Height

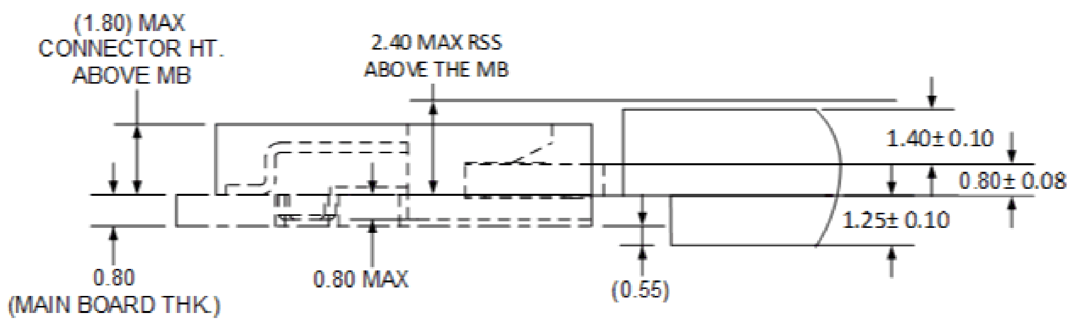


Figure 69. Stack-up Mid-mount (In-line) Double-sided (D3) Add-in Card ~~Module~~ for 1.5 Maximum Top-side Component Height

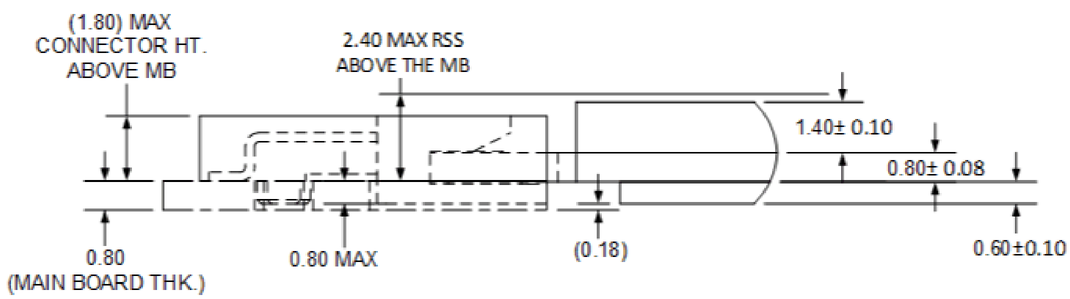


Figure 70. Stack-up Mid-mount (In-line) Double-sided (D4) Add-in Card ~~Module~~ for 1.5 Maximum Top-side Component Height

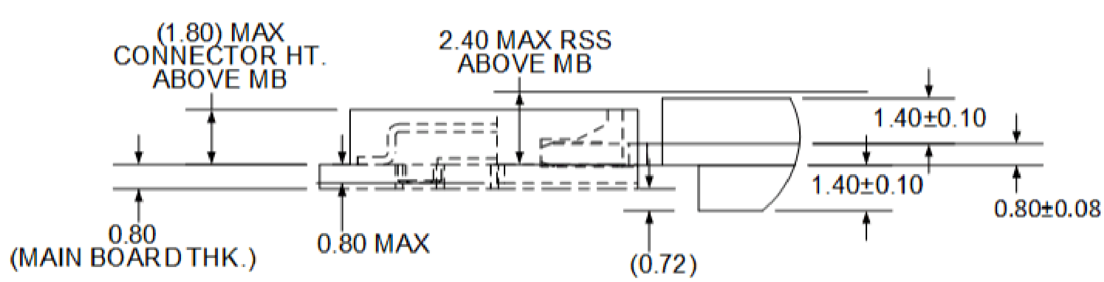


Figure 71. Stack-up Mid-mount (In-line) Double-sided (D5) Add-in Card ~~Module~~ for 1.5 Maximum Top-side and Bottom-side Component Height

2.4.8.4. Mid-mount Connector Layout Pattern

The layout footprint of the Mid-mount connector on the ~~platform~~ Platform side ~~Mother Board~~ is shown in the Figure 72. The land pattern includes all 75 pads although only up to 67 pads will be routed out while eight pads will be redundant as they are located where the Mechanical Key is located. Figure 72 shows the eight redundant pads of Key B as faded.

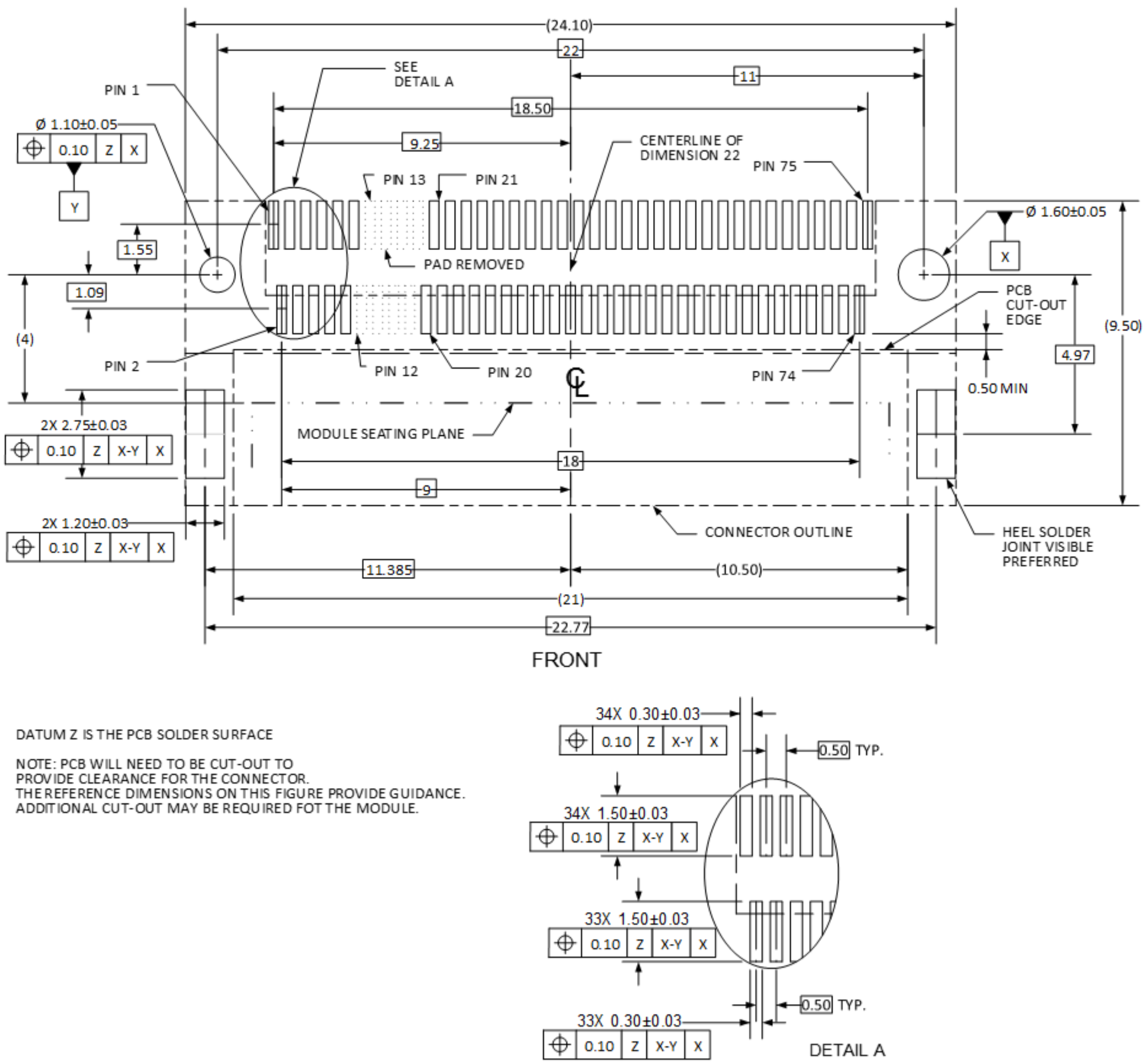


Figure 72. Example of Mid-mount ~~Motherboard~~Motherboard Land Pattern Diagram – Key B Shown

2.4.9. Connector Key Dimension

The width of the key is shown in Figure 73.

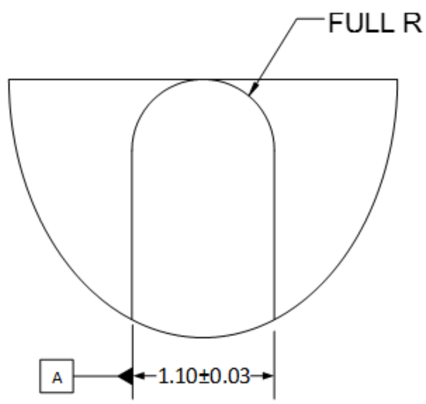


Figure 73. Connector Key

2.4.9.1. Host Connector Keying

The generic 75 position edge card connector on the mother~~-~~board side will incorporate a mechanical keying scheme to enable mating with only a matching keyed Add-in Card~~module~~. The mechanical key uses up eight pin locations (four on the top-side and four on the bottom-side). The generic 75-pin connector is able to accommodate 12 different mechanical Keys that are designated by a *Letter*. Each such Keyed connector will have 67 usable pins available but at alternate pin locations within the generic 75 pin locations.

The Mechanical Key mechanism will enable the following:

- Each Socket on the m~~M~~otherboard with a different mechanical key location to signify a different pinout and functionality of that particular socket
- To prevent wrongful insertion of an incompatible Add-in Card ~~module~~ into a wrong Socket connector on the m~~M~~otherboard, i~~. I~~ncluding the potential Add-in Card ~~module~~ inversion. This is required for Safety reasons.
- Multiple Add-in Card ~~module~~ key schemes that will enable insertion into more than one Socket

Mechanical keyed connectors that have their key locations within the first 49 pins (A, B, C, D, E, F, G, and H) ~~can~~ also accommodates the smaller 49 pin versions of the M.2 form factors like the Type 1630 Add-in Card~~board/module size~~. ~~These smaller modules, which probably contain less content and require the reduced pin count, could still be plugged into the same Motherboard keyed socket as their larger counterparts but enable module vendors a cost saving opportunity in the form of a smaller module for such simplistic solutions.~~

Figure 74 shows the relative location of the Mechanical Keys along the 75 positions. The Green and Blue marked areas are the locations of a reversed board showing that they do not coincide with the upright location of Keys. By assigning Key locations and making sure they are not interchangeable (upright or reversible), we end up with 12 distinct Keys.

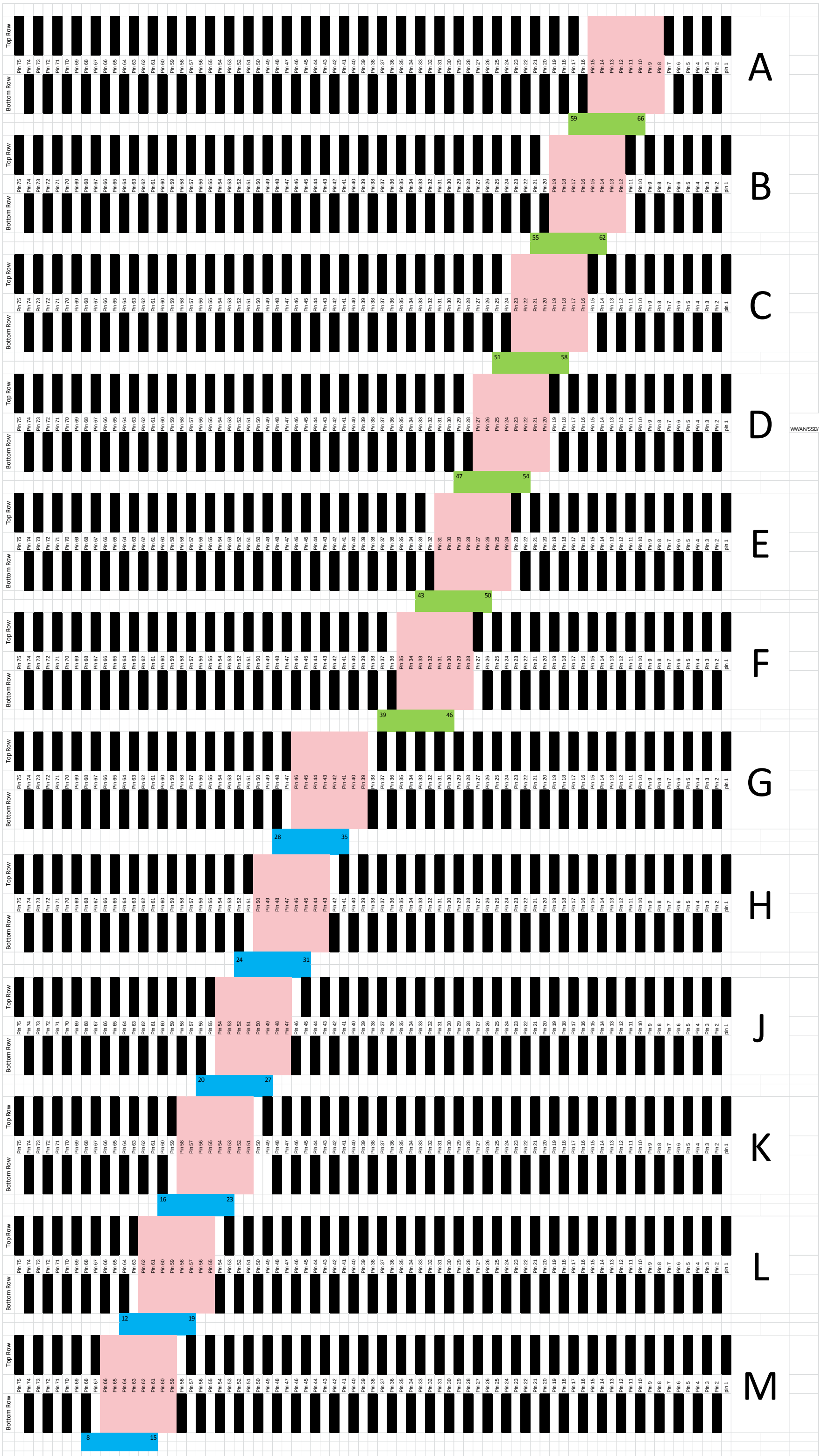


Figure 74. M.2 Connector Keying Diagram

This Connector Key/-Add-in Card ~~Module~~ Key system ~~can~~ enables some unique solutions in the form of a Dual Add-in Card ~~Module~~ key scheme. In such cases, an Add-in Card ~~module~~ with dual ~~module~~ keys would be able to plug into two different Keyed Connectors. But single ~~module~~ key Add-in Card ~~modules~~ intended for specific connector key would not be interchangeable. An example ~~can be seen~~is shown in Figure 75.

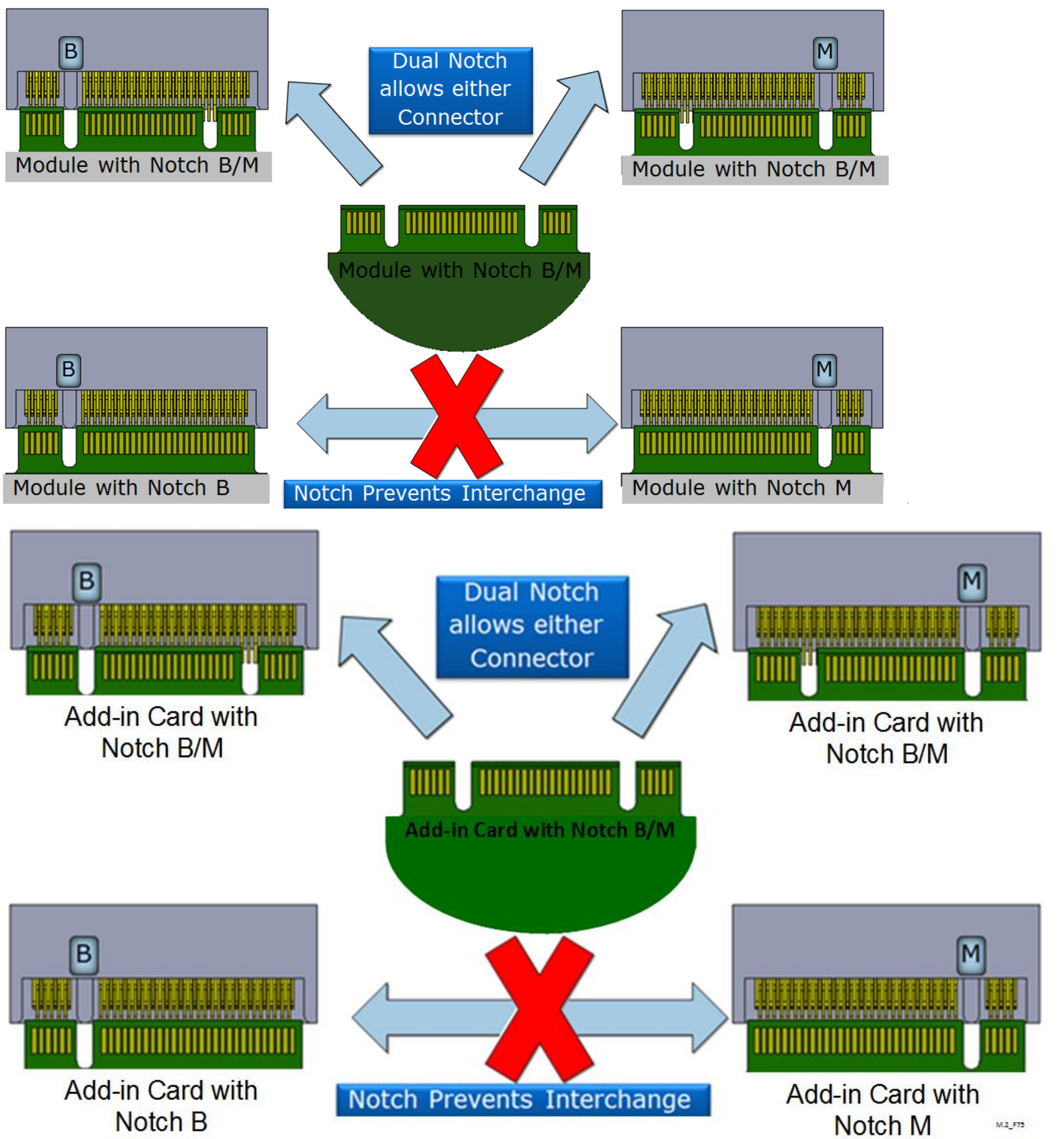


Figure 75. Dual ~~Module~~ Add-in Card Key Scheme Example

Such a scheme ~~could potentially be used to~~ enables ~~some modules~~ Add-in Cards to be plugged into two differently keyed connectors. For ~~exampl~~example; ~~e,~~ ~~an SSD Cache module that incorporates a dual module key could~~ it is possible to plug a SSD Cache Add-in Card that incorporates a dual Add-in Card key to ~~be plugged into~~ the WWAN/SSD/Other Socket 2 and also be plugged into a dedicated SSD Drive Socket 3. More details of such an example will be shown in the different Socket pinout section. This scheme is not limited to this example and ~~can be~~is implemented in those cases where the pinouts supported are able to support this sort of scheme.

2.5. Module Stand-off

The Add-in Card ~~modules~~ will need a mechanical retention at the end of the board. The Add-in Card ~~module~~ specifies a 5.5 mm diameter Keep-out zone at the end for attaching a screw. This section provides a guideline for using a M2 x 0.4 mm screw with a shoulder stand-off and a M3 x 0.5 mm screw. The guideline for the stand-off on the main board is recommending soldering down and assumed that the top-sided connectors are utilized. Alternatives are acceptable. The system will have to define the stand-off for utilizing the Mid-mount connectors.

2.5.1. Recommended Main Board Hole

The recommended plated-hole sizes for the main board are:

- Drill size 4.3 mm
- Finish size 4.2 ±0.075 mm
- Pad size 6.5 mm

2.5.2. Electrical Ground Path

The Add-in Card ~~module~~ Stand-off and mounting screw also serve as part of the Add-in Card ~~module~~ Electrical Ground path. The Stand-off should be connected directly to the ground (~~ground~~ GND) plane on the ~~platform~~Platform. So that when the Add-in Card ~~module~~ is mounted and the mounting screw is screwed on to hold the Add-in Card ~~module~~ in place, this will make the electrical ground connection from the Add-in Card to the ~~platform~~ Platform ground plane.

2.5.3. Thermal Ground Path

The stand-off must provide a Thermal Ground Path. The design requirements for thermal are a material with a minimum conductivity of 50 watts per meter Kelvin and surface area of 22 ~~Sq~~ mm^2 (see Figure 76).

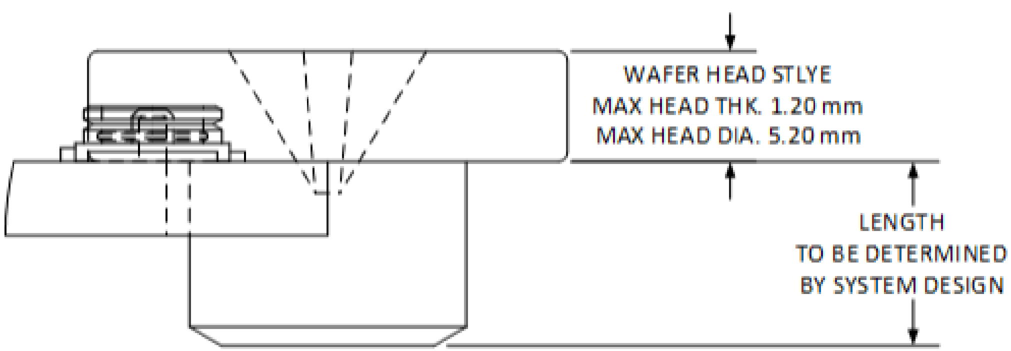


Figure 76. Mid-mount Add-in Card ~~Module~~ Mounting Interface

Top mount connectors will typically be complimented with a top mount stand-off. There are different types of stand-offs to coincide with the different height connectors as shown in the following figures:

- Figure 77. Single-sided Top Mount Solder-down Stand-off
- Figure 78. Elevated Single-sided Top Mount Solder Stand-off
- Figure 79. Low Profile Double-sided Top Mount Solder-down Stand-off
- Figure 80. Double-sided Top Mount Solder-down Stand-off
- Figure 81. Elevated Double-sided Top Mount Solder-down Stand-off

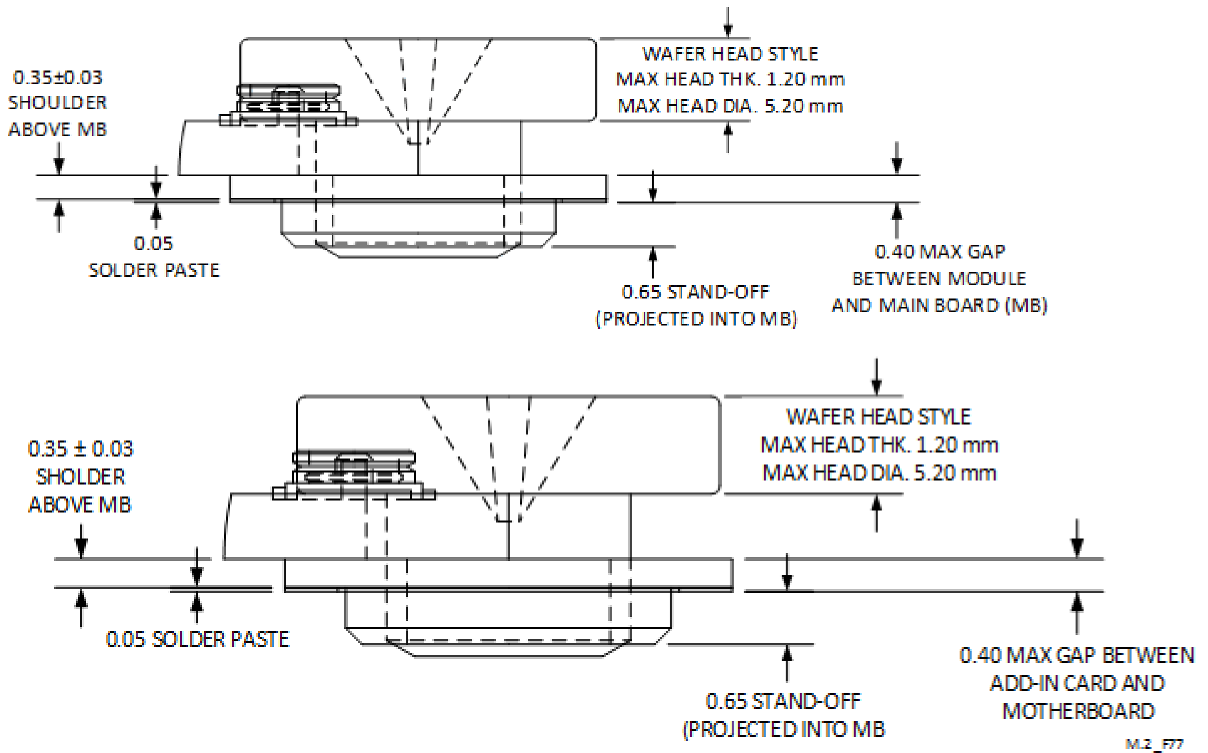


Figure 77. Single-sided Top Mount Solder-down Stand-off

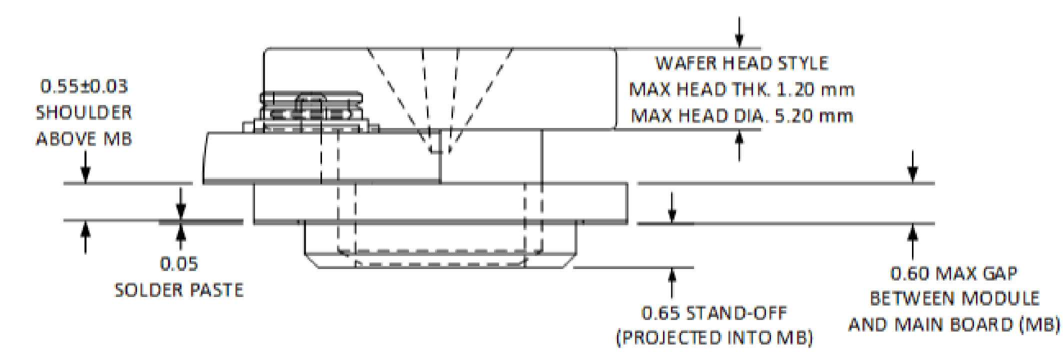


Figure 78. Elevated Single-sided Top Mount Solder Stand-off

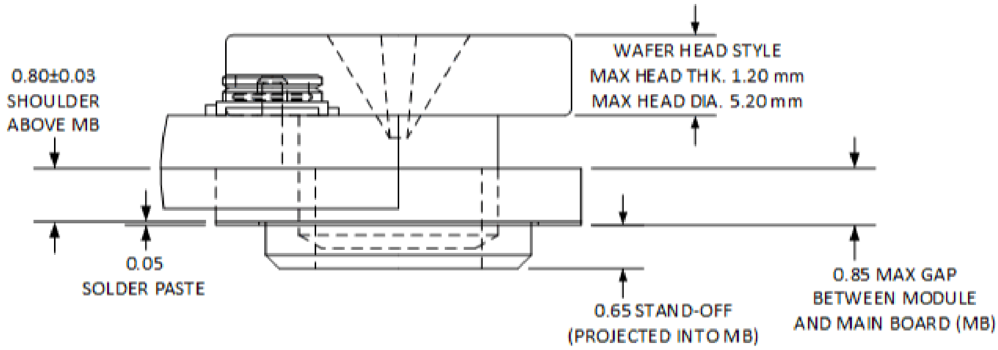


Figure 79. Low Profile Double-sided Top Mount Solder-down Stand-off

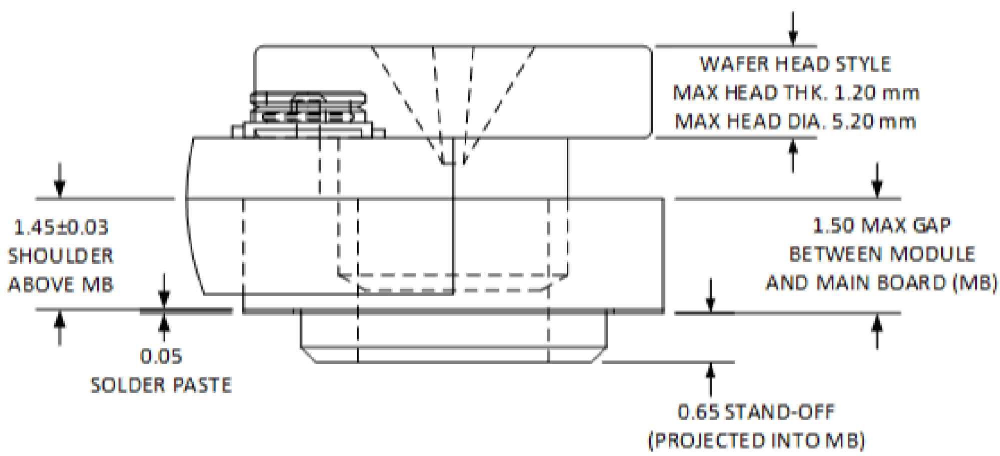


Figure 80. Double-sided Top Mount Solder-down Stand-off

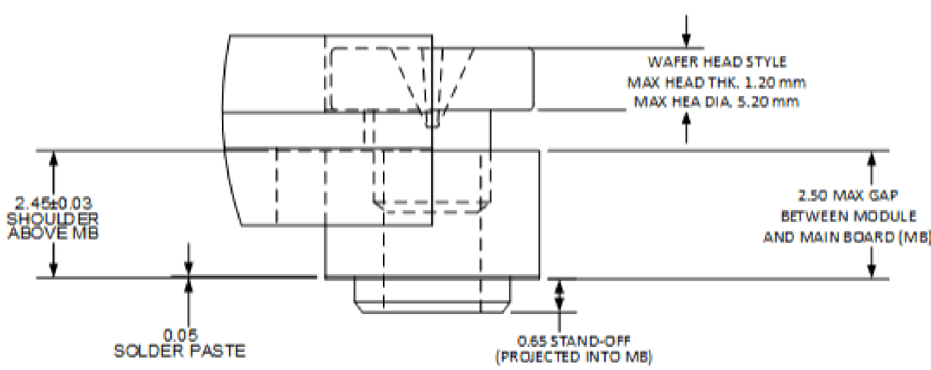


Figure 81. Elevated Double-sided Top Mount Solder-down Stand-off

2.5.4. Stand-off Guidelines

Figure 82 and Figure 83 provide a guideline for stand-offs for top-sided connectors.

2.5.4.1. Stand-off Guidelines Option 1

A flat stand-off is a board-level SMT component (see Figure 82) and has an M3 x 0.5 thread. The height of the stand-off is determined by what connector is used (see Table 14~~Table 14~~).

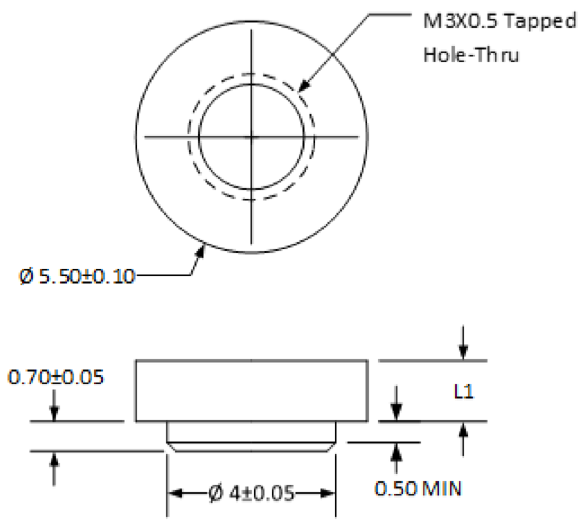


Figure 82. Flat Stand-off

Table 14. Stand-off Height Descriptor Table

Connector Height Descriptor	L1	L2
H2.3	0.35 ± 0.03	
H2.5	0.55 ± 0.03	
H2.8	0.80 ± 0.03	0.80 ± 0.03
H3.2	1.45 ± 0.03	1.45 ± 0.03
H4.2	2.45 ± 0.03	2.45 ± 0.03

Notes:

- Polyimide patch or tape required for vacuum pick-up
- Minimum thermal conductivity of 50 W/(mK) or greater
- Material = Steel
- Finish = Matte tin, 1.2 microns minimum average
- Tape and reel

2.5.4.2. Stand-off Guidelines Option 2

A shoulder stand-off is a board-level SMT component (see Figure 83) that has a M2 x 0.4 thread. The height of the stand-off is determined by what connector is used (see Table 14).

> **Note:** For a single-side connector, the shoulder stand-off is not recommended due to the insertion being nearly horizontal. The shoulder ~~could~~ makes insertion/removal of the ~~module~~ Add-in Card difficult due to clearing the cut-out.

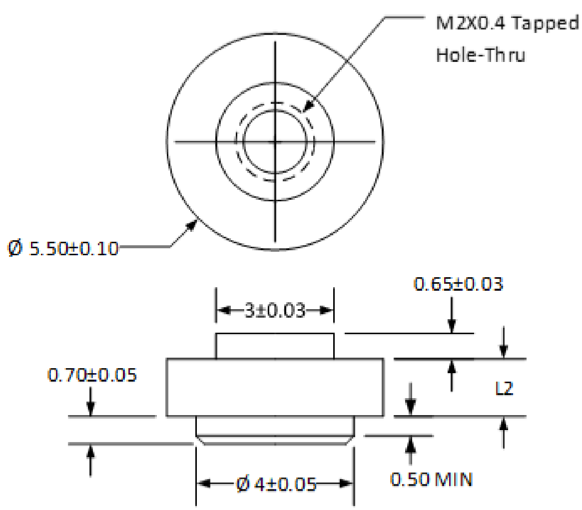


Figure 83. Shouldered Stand-off

2.5.5. Screw Selection Guideline

Screw selection consideration should be made according to the usage model. The tolerances of the connector, Add-in Card ~~module~~ and stand-off allow for a gap to exist between the seating plane and the contact, see Figure 84.

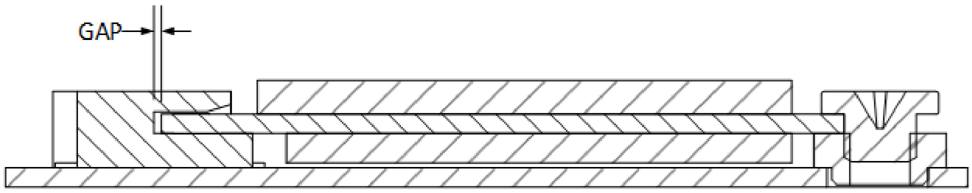


Figure 84. Screw Guidelines

2.5.5.1. Option 1, Wafer-head Style M3 Screw

Option 1 provides the guidelines for a wafer-head style M3 screw (see Figure 85). In using this screw type, the operator must be made aware that fully seating the Add-in Card ~~module~~ is required prior to securing the screw. The length is to be determined by the system design; 2 mm length supports all stand-off listed in Table 14. ~~Table 14~~

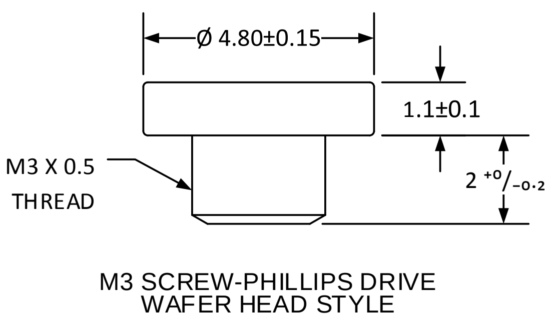


Figure 85. Wafer-head Style M3 Screw

2.5.5.2. Option 2, M3 Screw with Tapered Shaft

Option 2 provides the guidelines for a wafer-head style M3 screw (~~shown in~~see Figure 86) with a tapered shaft. In using this screw type, the taper shaft acts as a mechanical guide to minimize the gap. The length is to be determined by the system design; 2 mm length supports all stand-off listed in Table 14~~Table 14~~.

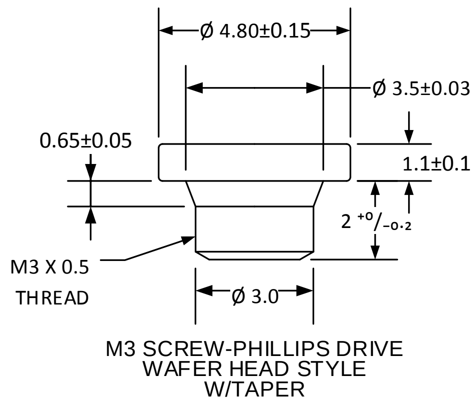


Figure 86. M3 Screw with Tapered Shaft

2.5.5.3. Option 3, Wafer-head Style M2 Screw

Option 3 provides the guidelines for a wafer-head style M2 screw (~~shown in~~see Figure 87). This screw is intended for use only with the shouldered stand-off. It is not recommended to be used alone as the cut-out size provides a strong potential of not seating properly. The Table 14.~~length is to be determined by the system design; 2 mm length supports all stand-off listed in Table 14~~

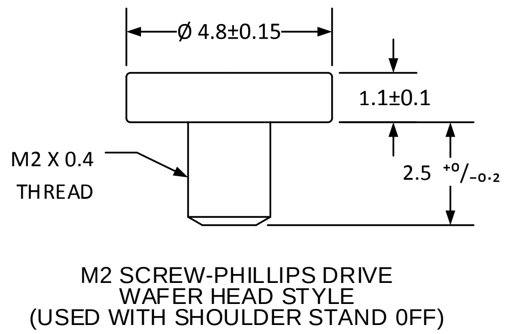
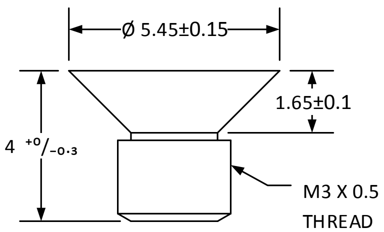


Figure 87. Wafer-head Style M2 Screw

2.5.5.4. Option 4, Flat-head Style M3 Screw

Option 4 provides the guidelines for a flat-head style M3 screw (~~shown in~~see Figure 88). In using this screw type the taper shaft acts as a mechanical guide to minimize the gap. Caution should be taken not to over torque the screw as it ~~could~~ damages the barrel on the plated cut-out. This screw does offer a low cost standard option providing a mechanism to mechanically control the gap. The length is to be determined by the system design; 2 mm length supports all stand-off listed in Table 14~~Table 14~~.



M3 SCREW-PHILLIPS DRIVE
FLAT HEAD STYLE

Figure 88. Flat-head Style M3 Screw

2.6. Thermal Guidelines for the M.2

The following thermal guidelines are intended to provide guidance to system designers and ~~module~~ Adapter designers using M.2 ~~modules~~. The thermal dissipation capability of any component or Adapter ~~module~~ is a function of the surrounding thermal environment. This guideline gives direction on assessing power dissipation capability for generic Adapters ~~modules~~ in certain classes of systems when no special thermal enhancement is applied to the Adapter ~~module~~. It also gives ~~module~~ the Adapter placement advice, although this advice should be considered informative rather than normative.

No specific maximum dissipation limits are given, as these limits are strongly system, use case, and system skin temperature dependent.

2.6.1. Objective

Establish dissipation response of Adapters~~modules~~, *Thermal Design Power*:

- By *generic* system environment (various categories defined; many assumptions)
- By card component type (generic packages, power maps defined)
- In presence of steady state dissipation in the rest of the system (use cases)

Based on limiting factors:

- Skin (exterior surface of casing) or display temperature limits

  OR
- Die maximum temperature, if this limit is reached first

2.6.2. Introduction to Thermal Management

This section addresses some of the key concepts for Adapter ~~module~~ thermal management. Because the connector forms a primary heat path to the main system board, thermal conditions on this board will provide a *background* temperature to an unpowered Adapter ~~module~~. Powering the Adapter ~~module~~ increases its temperature as well as that of the surroundings: not only the board on which the connector is mounted but also nearby elements such as system casing, display if present, batteries, and keyboard.

2.6.2.1. Thermal Design Power Definition

The definition of Thermal Design Power (TDP) is worst case average dissipation over a time duration. The time scales for fan systems are in the ~~one minute~~one-minute range. The time scales for fanless systems are in the ~~three minute~~three-minute range. Die thermal time constants are on the order of milliseconds, while power transients occur over even shorter time durations. However, since the thermal mass of the surrounding system is significant, the longer response time is of interest.

Note that this longer time scale dissipation is quite different from the maximum power, or even *normal* power drawn by the Adapter ~~module~~, as these tend to occur on a duty cycle with much shorter time scales than the TDP. In addition, any power sent out through an antenna would

subtract from the electrical power. The ~~thermal design power~~TDP is therefore always less than the maximum electrical power.

2.6.2.2. Skin Temperature Definition

For compact, portable systems, most of all the system's exterior surfaces (*casing* or *skin*) may be touched by the user. There are safety limits that apply to such surfaces, but the user's perception of *hot* is far lower than these safety limits. The perception is highly subjective and a matter of individual preference. Therefore, it is important for the system criteria to include a target temperature for various areas of the outer surface, and the conditions under which these should be met (ambient temperature, system activity, system orientation, area of system, size of hot spot, and so on). Some examples are given in this document, but these are intended only as examples and are not intended to cover the complete range of all possibilities. Careful consideration of the intended user and environment is imperative.

Note that although the system's exterior housing is often called *skin*, this refers only to the casing material and not to the human skin that may be touching it. In fact, the act of touching the casing ~~may~~ changes its temperature. The *perception* of temperature is less a matter of actual temperature than a question of the heat rate into the sensors embedded in human skin. This phenomenon is common in real life; ~~for example~~e.g., the perception of *hot* by a young child is very different from the perception by calloused or older hands. The perception aspect of the surface temperature leads to a variety of limit definitions.

2.6.2.3. Unpowered M.2 Adapter ~~Module~~ Temperature

The "background" or unpowered Adapter ~~module~~ temperature is a function of ~~motherboard~~motherboard *source* power, system environments, and other dissipation distributed around the system. This adiabatic or unpowered temperature is the **starting point for thermal ramp** as Adapter ~~module~~ switches from off or idle (~0 W) to powered. Skin temperatures in the vicinity of the Adapter ~~module~~ should be below the desired limits when the Adapter ~~module~~ is in this state.

Other characteristics of the unpowered Adapter ~~module~~ temperature are that it is nearly linear with **system power**; it is *specific to the individual system* (~~motherboard~~motherboard heat distribution, proximity of Adapters ~~modules~~ to other heat sources, cooling parameters, etc.); and the Adapter~~module~~'s own dissipation also raises temperatures of neighboring Adapters~~modules~~, ~~motherboard~~motherboard, and system skin. These surrounding temperature increases are also roughly linear with **Adapter ~~module~~ power**, and vary with Adapter ~~module~~ characteristics (size, heat distribution, heat paths to surroundings) and are also specific to individual system design parameters. Therefore, these characteristics should be quantified for each system design. By extension, the results given in this document are meant to provide only an example of the approach to determining the dissipation response of Adapters~~modules~~.

2.6.2.4. System Skin Temperature—Fan-based System

In a system that includes a fan, major heat sources are cooled by a thermal solution if needed and a fan. The air flow path is determined by vent placement, fan speed, obstructions, and so on. The cooling strategy should seek to maximize air flow for a given fan speed by reducing the pressure

drop though the air path. As a general rule, sources of pressure drop that do not also accomplish a cooling task should be avoided as much as possible.

As skin temperature is a local heat density effect, it is important to flush air through the gap between skin and the Adapter~~module~~. This will not completely prevent the Adapter ~~module~~ heating the skin, but allows more of the Adapter ~~module~~ heat to be exhausted from the system without having to pass through the casing. The Adapter ~~module~~ dissipation limit depends on air speed, but the air speed depends on the gap size, vent placement, fan speed, and other parameters in the flow path both upstream and downstream.

Another approach to reducing skin temperature over Adapters ~~modules~~ is to include a long, narrow vent between high heat areas and the Adapter~~module~~. The vent ~~can~~ acts as a thermal break for the Adapter ~~module~~, but it will reduce the area of outer casing available for cooling the high heat components.

In some systems, the fan flow rate is severely restricted by the proximity of the system casing or other elements. The fan's inlet side is obstructed by the resulting narrow gap, and this ~~may~~ alters the fan's characteristic curve from published data. Therefore, care should be taken to evaluate the true fan flow rate as installed in the system. In such systems, the low fan flow will exhaust proportionately less heat, leaving the remainder to pass through the casing as for fanless systems, below.

2.6.3. System Skin Temperature—Fanless System

All heat dissipated inside the system, by any heat source, must pass *through* the casing (which has minimal temperature gradient through the material thickness, even if resin based) and dissipate off the exterior surface to the environment by radiation and natural convection. Thus, the surface temperature is *total system power* and *surface area dependent*. High emissivity of the outer surface in the long-infrared range, ~~for example~~e.g., by paint, anodize, or resin coating, is helpful for decreasing surface temperature. A metal casing produces more uniform skin temperature than resins, but has more restrictive temperature limits. In most cases the heat spreading ability of the metal is beneficial to system cooling despite the lower temperature limits.

2.6.4. Examples of Dissipation (TDP) Response of Adapters~~Modules~~

Examples of dissipation (TDP) response of Adapters ~~modules~~ in systems ~~can be found~~are given in section 6.5, Thermal Guideline Annex. The general trend is that the skin temperature of a system is dominated by the system's use case and layout—changes in the Adapter ~~module~~ TDP locally perturbs the skin temperature. Higher levels of fan ventilation reduce the sensitivity of local skin temperature to Adapter ~~module~~ TDP.

3

3. Electrical Specifications

This chapter covers the electrical specifications for the PCI Express M.2 family of Adapters~~modules~~.

> All pinouts tables in this section are written from the Adapter ~~module~~ point of view when referencing signal directions.

3.1. Connectivity Socket 1 Adapter ~~Module~~ Interface Signals

Table 15 applies to both Socket 1 SDIO-based and Socket 1 Display Port-based pinout versions.

Table 15. Socket 1 System Interface Signals and Voltage Table

Signal Group	Signal	I/O	Description	Voltage
Power	~~+~~3.3 V (4 pins)	I	3.3 V source.	3.3 V
	GND		Return current path.	0 V
WiFi-SDIO	SDIO_CLK	I	SDIO 3.0 Clock, 1.8 V for SDR25 ~~&~~and DDR50 mode.	1.8 V
	SDIO_CMD	I/O	SDIO Command Interface, 1.8 V for SDR25 and DDR50 mode.	1.8 V
	SDIO_DATA[0:3]	I/O	Four lines for SDIO data exchange, 1.8 V for SDR25 ~~&~~and DDR50 mode.	1.8 V
	SDIO_ WAKE#	O	SDIO sideband Wake. Note: In band SDIO wake is not used for non-active modes~~, Active Low. Require pull up on the host side (recommended 15kΩ to 100kΩ).~~. Active Low; Required pull up on the host side (recommended 15 kΩ to 100 kΩ).	1.8 V

Signal Group	Signal	I/O	Description	Voltage
	SDIO_ RESET#	I	SDIO sideband GPIO pin to enable/disable (reset) the Wi-Fi function. ~~Platform~~Platform firmware is required to assert/de-assert this pin on every boot (warm and cold). ~~–~~The Wi-Fi device ~~may~~ uses 0.5 mW to 1 mW in reset, Active Low.	1.8 V
UART	UART_RXD	I	UART Receive Data connected to TXD on the P~~p~~latform.	1.8 V
	UART_TXD	O	UART Transmit Data connected to RXD on the P~~p~~latform.	1.8 V
	UART RTS	O	UART Ready To Send connected to CTS on the P~~p~~latform.	1.8 V
	UART CTS	I	UART Clear To Send connected to RTS on the P~~p~~latform.	1.8 V
	UART_WAKE#	O	UART sideband used to Wake up P~~p~~latform. Open Drain, Active Low. Require pull up on the host side (recommended 15 KΩ to 100 KΩ).	3.3 V
PCM(I2S)	PCM_CLK / I²S SCK	I/O	PCM Clock/ I²S Continuous Serial Clock (SCK).	1.8 V
	PCM_SYNC / I²S WS	I/O	PCM synchronous data SYNC/ I²S Word Select.	1.8 V
	PCM_IN / I²S SD_IN	I	PCM synchronous data INput/ I²S Serial Data IN.	1.8 V
	PCM_OUT / I²S SD_OUT	O	PCM synchronous data OUTput/ I²S Serial Data OUT.	1.8 V
PCIe (up to two instances)	PERp0, PERn0/ PETp0, PETn0	I/O	PCIe TX/RX Differential signals defined by the *PCI Express Card Electromechanical Specification*~~PCIe 3.0 specification~~.	
	REFCLKp0/ REFCLKn0	I	PCIe Reference Clock signals (100 MHz) defined by the *PCI Express Card Electromechanical Specification*~~PCIe 3.0 specification~~.	
	PERST0#	I	PCIe Reset is a functional reset to the Adapter ~~Add-In card~~ as defined by the *PCI Express Mini Card Electromechanical Specification*~~PCIe Mini CEM specification~~.	3.3 V
	CLKREQ0#	I/O	Clock Request is a reference clock request signal as defined by the *PCI Express Mini Card Electromechanical Specification*~~PCIe Mini CEM specification~~; a~~A~~lso used by L1 PM Substates. Open Drain with pull up on P~~p~~latform; Active Low.	3.3 V

Signal Group	Signal	I/O	Description	Voltage
	PEWAKE#/ OBFF	I/O	PCIe WAKE#. Open Drain with pull-up on P~~p~~latform. Active Low when used as PEWAKE#. When the Adapter ~~add-in module~~ supports wakeup, this signal is used to request that the system return from a sleep/suspend state to service a function initiated wake event. When the ~~add-in~~ Adapter ~~module~~ supports OBFF mechanism, the signal is used by the system to indicate OBFF or CPU Active State transitions.	3.3 V
USB	USB D+, USB D-	I/O	USB Data ± Differential serial data interface compliant to the *USB 2.0 Specification*.	
I2C	ALERT#	O	IRQ line to host processor; Open Drain with pull up on ~~platform~~Platform; Active Low.	1.8 V
	I2C_CLK	I	I2C clock input from host. Open Drain with pull up on ~~platform~~Platform.	1 8 V
	I2C_DATA	I/O	I2C data. Open Drain with pull up on ~~platform~~Platform.	1.8 V
Display Port	DP_HPD	I or O	Hot Plug Detect. Direction is determined by DP_MLDIR.	3.3 V
	DP_MLDIR	I/O	Display Port data interface direction.	0 V/ 3.3 V / NC
	DP_AUXp/DP_AUXn	I/O	Auxiliary Channel; Bidirectional half-duplex AUX channel, DisplayPort v1.2, AUX channel 1 Mbit/s. Signal direction dictated by DP_MLDIR.	
	DP_ML0p/DP_ML0n, DP_ML1p/DP_ML1n, DP_ML2p/DP_ML2n, DP_ML3p/DP_ML3n,	I or O	Up to 4 Lane; Effective data rate 1.296 Gb/s, 2.16 Gb/s or 4.32 Gb/s per lane. DisplayPort main link data interface: four unidirectional differential pairs, signal direction dictated by MLDIR.	
Communication-specific Signals	SUSCLK	I	Suspend Clock is a 32.768 kHz clock supply input that is provided by ~~platform~~ Platform to enable the Adapter ~~add-in card~~ to enter reduce power consumption modes. SUSCLK duty cycle is permitted to be as low as 30% or as high as 70%. The tolerance for this clock is ±100 ppm~~SUSCLK will have a duty cycle that can be as low as 30% or as high as 70%. Accuracy will be up to 200 ppm~~.	3.3 V

Signal Group	Signal	I/O	Description	Voltage
	W_DISABLE1# W_DISABLE2#	I	Active low, debounced signal when applied by the system it will disable radio operation on the Adapter ~~add-in cards~~ that implement radio frequency applications. When implemented, these signals require a pull-up resistor on the Adapter~~card~~.	3.3 V
	LED_1# LED_2#	O	Open drain, active low signal. These signals are used to allow the Adapters ~~add-in card~~ to provide status indicators via LED devices that will be provided by the system.	3.3 V
	COEX_RXD COEX_TXD COEX_3	I O I/O	Coexistence between WiFi+BT and WWAN on Socket 2. UART TxD and RxD signals per BT-SIG coexistence protocol + an undefined signal.	1.8 V
	TX_BLANKING	I	TX_BLANKING GNSS Aiding signal from WWAN (see S~~s~~ection 3.2.11.3.1~~, GNSS Signals~~ for more information).	1.8 V
	SYSCLK	I	SYSCLK GNSS Aiding signal from WWAN (see S~~s~~ection 3.2.11.3.1~~, GNSS Signals~~ for more information).	1.8 V
NFC-UIM Signals	UIM_POWER_SRC/ GPIO_1	I	UICC power out from BB PMU.	Per ISO 7816 Spec~~ification~~
	UIM_POWER_SNK	O	NFC PMU power to the UICC.	
	SWP	I/O	UICC Secure element.	

3.1.1. Power Sources and Grounds

PCI Express M.2 Socket 1 utilizes a single 3.3 V power sources. The voltage source, ~~+~~3.3 V, is expected to be available during the system's stand-by/suspend state to support wake event processing on the communications card.

Some of the higher frequency signals require additional isolation from surrounding signals using the concept of ~~interleavin~~interleaving ~~g ground (~~GND~~)~~ pins separating signals within the connector. These pins should be treated as a normal ground pin with connections immediately made to the ~~ground~~ GND planes within a card design.

3.1.2. PCI Express Interface

The PCI Express interface supports a x1 PCI Express interface (one Lane). A Lane consists of an input and an output high-speed differential pair. Also supported is a PCI Express reference clock. Refer to the *PCI Express Base Specification* for more details on the functional requirements for the PCI Express interface signals.

IMPLEMENTATION NOTE: Lane Polarity

By default, the PETp0 and PETn0 pins (the transmitter differential pair of the connector) ~~shall be~~are connected to the PCI Express transmitter differential pair on the system board and to the PCI Express receiver differential pair on the PCI Express M.2 Adapter~~Card add-in card~~. ~~Similarly~~Similarly, by default, the PERp0 and PERn0 pins (the receiver differential pair of the connector) ~~shall be~~are connected to the PCI Express receiver differential pair on the system board and to the PCI Express transmitter differential pair on the PCI Express M.2 Adapter~~Card add-in card~~.

However, the **p** and **n** connections ~~may be~~may be reversed to simplify PCB trace routing and minimize vias if needed. All PCI Express receivers incorporate automatic Lane polarity inversion as part of the Link initialization and training and will correct the polarity independently on each Lane.

Refer to ~~section 4.2.4 of~~ the *PCI Express Base Specification* for more information on Link initialization and training.

IMPLEMENTATION NOTE: Link Power Management

PCI Express M.2 Adapters ~~add-in cards~~ that implement PCI Express-based applications are required by the *PCI Express Base Specification* to implement Link power management states, including support for the L0s and L1 (in addition to the primary L0 and L3 states). For PCI Express M.2 ~~Card~~ implementations, Active State Power Management for both L0s and L1 states ~~shall also be~~are enabled by default. Refer to ~~Section 5.4 of~~ the *PCI Express Base Specification* for more information regarding Active State Power Management.

Socket 1 pinouts has provision for an additional PCI Express lane indicated by the suffix 1 to the signal names. These additional PETx1 and PERx1 signal sets ~~can~~ serve as the second Lane to the original PCI Express interface, or alternatively, they ~~can be~~are complimented with a second set of REFCLKx1 and a set of Auxiliary Signals on the adjacent Reserved pins to form a complete second PCI Express x1 interface.

3.1.3. PCI Express Auxiliary Signals

The auxiliary signals are provided on the system connector to assist with certain system level functionality or implementation. These signals are not required by the PCI Express architecture, but may be required by specific implementations such as a PCI Express M.2 Device. The high-speed signal voltage levels are compatible with advanced silicon processes. The optional low speed signals are defined to use the ~~+~~3.3 V supply, as it is the lowest common voltage available. Most ASIC processes have high voltage (thick gate oxide) I/O transistors compatible with ~~+~~3.3 V. The use of the ~~+~~3.3 V supply allows PCI Express signaling to be used with existing control bus structures, avoiding a buffered set of signals and bridges between the buses.

The PCI Express M.2 Device and system connectors support the auxiliary signals that are described in the following sections.

3.1.3.1. Reference Clock

The REFCLKp/REFCLKn signals are used to assist the synchronization of the device's PCI Express interface timing circuits. Availability of the reference clock ~~may be~~is gated by the CLKREQ# signal as described in section 3.1.3.2. When the reference clock is not available, it will be in the *parked* state. A parked state is when the clock is not being driven by a clock driver and both REFCLKp and REFCLKn are pulled to ground by the ~~ground~~ GND termination resistors. Refer to the *PCI Express Card Electromechanical Specification* for more details on the functional and tolerance requirements for the reference clock signals.

3.1.3.2. CLKREQ# Signal

The CLKREQ# signal is an open drain, active low signal that is driven low by the PCI Express M.2 device to request that the PCI Express reference clock be available (active clock state) in order to allow the PCI Express interface to send/receive data. Operation of the CLKREQ# signal is determined by the state of the Enable Clock Power Management bit in the Link Control Register (offset 010h). When the Enable Clock Power Management bit is disabled, the CLKREQ# signal ~~shall~~ must be asserted at all times whenever power is applied to the device, with the exception that it ~~may~~

is permitted to be de-asserted during L1 PM Substates. When the Enable Clock Power Management bit is enabled, the CLKREQ# signal ~~may be~~ is permitted to be de-asserted during the L1 Link state.

The CLKREQ# signal is also used by the L1 PM Substates mechanism. In this case, CLKREQ# ~~can be~~is asserted by either the system or the device to initiate an L1 exit. ~~See~~ Refer to the *PCI Express Base Specification* for details on the functional requirements for the CLKREQ# signal when implementing L1 PM Substates.

Whenever dynamic clock management is enabled and when a device stops driving CLKREQ# low, it indicates that the device is ready for the reference clock to transition from the active clock state to a parked (not available) clock state. Reference clocks are not guaranteed to be parked by the host system when CLKREQ# gets de-asserted and ~~the~~ devices ~~shall~~ must be tolerant of an active reference clock even when CLKREQ# is de-asserted by the device.

The device must drive the CLKREQ# signal low during power up, whenever the device is reset, and whenever the device requires the reference clock to be in the active clock state. Whenever PERST# is asserted, including when the device is not in D0, CLKREQ# ~~shall~~ must be asserted.

It is important to note that the PCI Express device must delay de-assertion of its CLKREQ# signal until it is ready for its reference clock to be parked. The device must be able to assert its clock request signal, whether or not the reference clock is active or parked, when the device needs to put its Link back into the L0 Link state. Finally, the device must be able to sense an electrical idle break on its up-stream-directed receive port and assert its clock request, whether or not the reference clock is active or parked.

The assertion and de-assertion of CLKREQ# are asynchronous with respect to the reference clock.

Devices that do not implement a PCI Express interface ~~shall~~ must leave this CLKREQ# output unconnected.

CLKREQ# has additional electrical requirements over and above ~~standard~~ conventional open drain signals that allow it to be shared between devices that are powered off and other devices that ~~may be~~are powered on. The additional requirements include careful circuit design to ensure that a voltage applied to the CLKREQ# signal network never causes damage to a component even if that particular component's power is not applied.

Additionally, the device must ensure that it does not pull CLKREQ# low unless CLKREQ# is being intentionally asserted in all cases; including when the related function is in ~~$D3_{cold}$~~$D3_{cold}$. This means that any component implementing CLKREQ# must be designed such that:

- Unpowered CLKREQ# output circuits are not damaged if a voltage is applied to them from other powered "wire-ORed" sources of CLKREQ#.
- When power is removed from its CLKREQ# generation logic, the unpowered output does not present a low impedance path to ground or any other voltage.

These additional requirements ensure that the CLKREQ# signal network continues to function properly when a mixture of powered and unpowered components have their CLKREQ# outputs wire-ORed together. It is important to note that most commonly available open drain and tri-state buffer circuit designs used "as is" do not satisfy the additional circuit design requirements for CLKREQ#.

3.1.3.2.1. Dynamic Clock Control

If Clock Power Management is enabled in Link Control Register ~~After~~ after a PCI Express device has powered up and ~~whenever~~ its upstream link enters the L1 link state, it ~~shall~~ must allow its reference clock to be turned off (put into the parked clock state). To accomplish this, the device de-asserts CLKREQ# (high) and must allow that the reference clock will transition to the parked clock state within a delay (T_{CRHoff}). Figure 89 shows the CLKREQ# clock control timing diagram.

To exit L1, the device must assert CLKREQ# (low) to re-enable the reference clock. After the device asserts CLKREQ# (low) it must allow that the reference clock will continue to be in the parked clock state for a delay (T_{CRLon}) before transitioning to the active clock state. The time that it takes for the device to assert CLKREQ# and for the system to return the reference clock to the active clock state are serialized with respect to the remainder of L1 recovery. This time must be taken into account when the device is reporting its L1 exit latency.

When the PCI Express device supports, and is enabled for, Latency Tolerance Reporting (LTR), the device must allow that the reference clock transition to the active clock state ~~may be~~is additionally delayed by the system up to a maximum value consistent with requirements for the LTR mechanism. During this delay, the reference clock must remain parked. When exiting the parked state following the delay, the clock must be stable and valid within 400 ns.

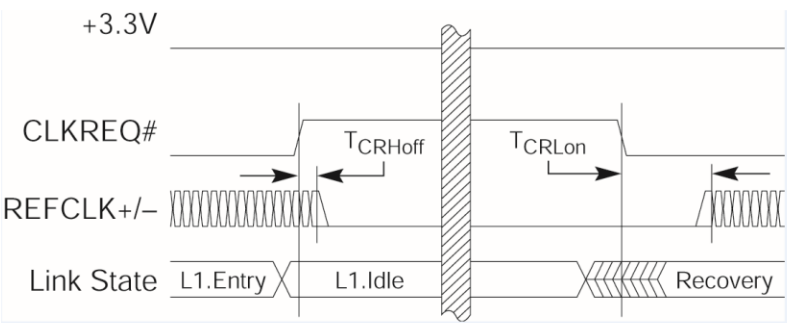


Figure 89. CLKREQ# Clock Control Timings

All links attached to a PCI Express device must complete a transition to the L1.Idle state before the device ~~can~~ de-asserts CLKREQ#. The device must assert CLKREQ# when it detects an electrical idle break on any receiver port. The device must assert CLKREQ# at the same time it breaks electrical idle on any of its transmitter ports in order to minimize L1 exit latency. See Table 16 for CLKREQ# clock control timing.

Table 16. Power-up CLKREQ# Timings

Symbol	Parameter	Min	Max	Units	Note
T_{CRHoff}	CLKREQ# de-asserted high to clock parked	0		ns	
T_{CRLon}	CLKREQ# asserted low to clock active		400*	ns	See Note

Note: ~~*~~ T_{CRLon} is allowed to exceed this value when LTR is supported and enabled for the device.

There is no maximum specification for T_{CRHoff} and no minimum specification for T_{CRLon}. This means that the system is not required to implement reference clock parking or that the system is permitted to ignore device's request to park reference clock. ~~that the implementation may not always act on a device de-asserting CLKREQ#.~~ A device should also de-assert CLKREQ# when its link is in L2 or L3, much as it does during L1.

3.1.3.3. Clock Request Support Reporting and Enabling

Support for the CLKREQ# dynamic clock protocol must be reported using bit 18 in the PCI Express Link Capabilities register (offset 00Ch). To enable dynamic clock management, bit 8 of the Link Control register (offset 010h) is provided. By default, the device ~~shall~~ must enable CLKREQ# dynamic clock protocol upon initial power up and in response to any warm reset by the host system. System software ~~may~~ subsequently disables this feature as needed. Refer to the *PCI Express Base Specification*~~,~~ for more information regarding these bits.

3.1.3.4. PERST# Signal

- The PERST# signal is de-asserted to indicate when the system power sources are within their specified voltage tolerance and are stable.
- PERST# must be used to initialize the card functions once power sources stabilize.
- PERST# is asserted when power is switched off and also ~~can be~~is used by the system to force a hardware reset on the card.
- System ~~may~~ must use PERST# to cause a warm reset of the ~~add-in card~~Adapter.
- PERST# is asserted in advance of the power being switched off in a power-managed state like S3.
- PERST# is asserted when the power supply is powered down, but without the advanced warning of the transition.

3.1.3.5. PEWAKE# Signal

PCI Express M.2 Cards must implement PEWAKE# if the card supports either the wakeup function or the OBFF mechanism. Refer to the WAKE# signal definition section in the *PCI Express Card Electromechanical Specification* for more details on the functional requirements for the PEWAKE# signal.

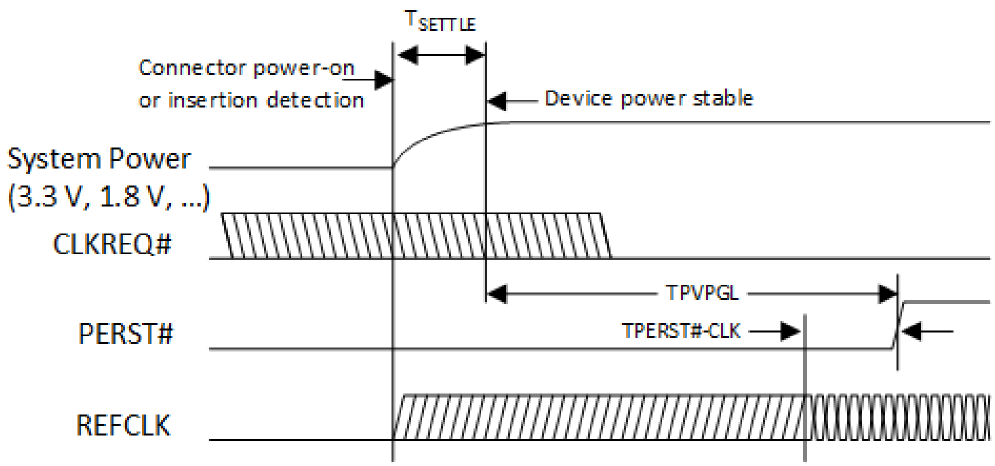
> **Note** The PEWAKE# signal in ~~the M.2~~this ~~S~~specification is referring to the PCIe WAKE# signal indicated in other PCIe-related specifications. The PE name prefix is intended to distinguish between this PCIe WAKE# and other host interface WAKE signals included in ~~the M.2~~this ~~S~~specification.

3.1.4. Power-up Timing

Figure 90 shows an overview of the M.2 Adapter ~~device~~ power-up sequence for an Adapter ~~module~~ powered from the system power rail. Figure 91 shows an overview of the M.2 power-up sequence for an Adapter ~~module~~ powered by a direct ~~V_{BAT}~~V_{BAT} connection. In case of a direct V_{BAT} connection, the de-assertion of FULL_CARD_POWER_OFF# triggers start of the Adapter ~~module~~ power-up sequence. It is assumed that V_{BAT} will be within its specified voltage range (see ~~S~~section 4.3~~, Power~~)

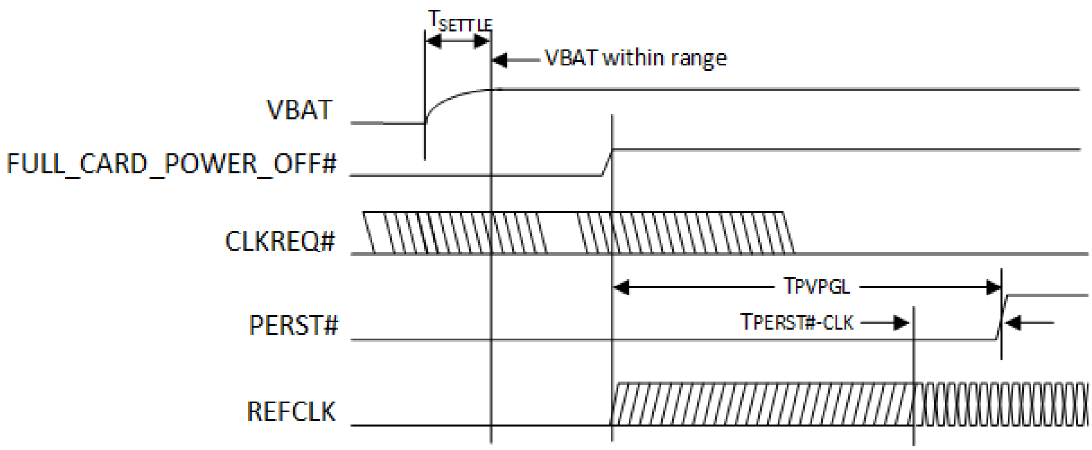
well before FULL_CARD_POWER_OFF# becomes de-asserted. See section 3.2.11.1, REF _Ref358191055 \h * MERGEFORMAT FULL_CARD_POWER_OFF#, for details about the FULL_CARD_POWER_OFF# signal.

Table 17 lists the power-up timing variable values.



Note: T_{settle} is the time it takes all Power Rails to reach their minimum operating voltage (i.e., from all Power Rails at 0 V to the last Power Rail to reach its minimum valid operating voltage). All other PCI Express related timing events will begin once all of the Power Rails have reached their minimum operating voltage. For example, a typical Adapter ~~module~~ with a load capacitance of 330 µF and a 200 mA Soft-Start current limited ramp on the 3.3 V power rail, should settle within 5 ms.~~s.~~

Figure 90. Power-up Timing Sequence for an Adapter ~~Module~~ Powered from System Power Rail



Note: T_{settle} is the time it takes all Power Rails to reach their minimum operating voltage (i.e., from all Power Rails at 0 V to the last Power Rail to reach its minimum valid operating voltage). All other PCI Express related timing events will begin once all of the Power Rails have reached their minimum operating voltage. For example, a typical Adapter with a load capacitance of 330 µF and a 200 mA Soft-Start current limited ramp on the 3.3 V power rail, should settle within 5 ms.

Figure 91. Power-up Timing Sequence for ~~a Module~~an Adapter Powered by a Direct V_{BAT} Connection

Table 17. Power-up Timing Variables

Symbol	Parameter	Min	Max	Units
T_{PVPGL}	Power Valid* to PERST# input inactive (see Note)	Implementation specific; recommended 50 ms		ms
$T_{PERST\#-CLK}$	REFCLK stable before PERST# inactive	100		µs
Note: *Power Valid when all the voltage supply rails have reached their respective V_{min}.				

3.1.4.1. PERST# Power-up Timing

The host ~~shall~~ must delay de-assertion of PERST# for a period of time (T_{PVPGL}) after power is stable on the device (see Figure 90 and Figure 91). See section 3.1.3.4, *PERST# Signal*, for further details on PERST#.

The *PCI Express Base Specification* ~~(Conventional Reset)~~ requires that a PCI Express device must be in the LTSSM Detect state within 20 ms of PERST# being de-asserted and ready for Configuration Requests within 120 ms of PERST# being de-asserted.

The value of T_{PVPGL} is left as implementation specific, with a recommended value as a guideline. In considering the value of T_{PVPGL}:

- Device and host implementers should consult PCI Express Reset Rules and ~~platform~~ Platform BIOS and OS requirements governing device readiness timing requirements following the de-assertion of PERST#.

- Host implementers should consult device vendors for their T_{PVPGL} values, based on VENDOR DEFINED device startup requirements.

3.1.4.2. REFCLK Power-up Timing

The host ~~shall~~ must ensure that the reference clock is in the active clock state for at least a period of time specified by $T_{PERST\#\text{-}CLK}$, prior to PERST# de-assertion. See section 3.1.3.1, Reference Clock, for further details on REFCLK.

3.1.4.3. CLKREQ# Power-up Timing

See section 3.1.3.2, *CLKREQ# Signal*, for details on CLKREQ#.

3.1.5. USB Interface

The USB interface supports USB 2.0 in all three modes (Low Speed, Full Speed, and High Speed). Because there is not a separate USB-controlled voltage bus, USB functions implemented on a PCI Express M.2 Adapter ~~Card add-in card~~ are expected to report as self-powered devices. All enumeration, bus protocol, and bus management features for this interface are defined by *Universal Serial Bus Specification*, Revision 2.0.

USB-based M.2 Adapters ~~Cards~~ that implement a wakeup process are required to use the in-band wakeup protocol (across the USB_D+/USB_D– pins) as defined in the *Universal Serial Bus Specification*.

3.1.6. Display Port Interface

The DisplayPort interface supports a full-featured implementation as defined in the referenced *DisplayPort Standard Specification*. A full four lane implementation of the main link, the auxiliary channel, and hot plug detect (DP_HPD) is supported. Additionally, a system level signal, DP_MLDIR, is provided to assist in configuration of the ~~platform~~ Platform when a Display-M.2 Adapter ~~Card~~ is installed.

3.1.6.1. DP_HPD

The DP_HPD signal connects to the standard Hot Plug Detect signal of the Display Port interface. The intent of this signal is to indicate to the DisplayPort source that an active display is connected. The logical direction of DP_HPD is determined by the state of DP_MLDIR.

For a wireless display application, DP_HPD being asserted ~~shall also be~~is an indication that the wireless link between the system and the remote display is fully operational. When DP_HPD is asserted, the host system software will know to locate and configure the remote display.

3.1.6.2. DP_MLDIR

The DP_MLDIR signal indicates the functional direction of the DisplayPort data and auxiliary interfaces on an M.2 Adapter~~Card~~; ~~i.e~~e.g., as a sink or source of the display-related interfaces. Based

on the specific DisplayPort capabilities of the M.2 Adapter ~~Card~~ installed in the socket, the DP_MLDIR signal termination on the card ~~shall~~ must be as defined in Table 18.

For the M.2 Adapter ~~Card~~ that offers bi-directional DisplayPort capabilities, the mechanism for configuring the direction of the display interface is application and/or product-specific and not defined by this specification.

Table 18. DP_MLDIR Pin Termination

Display-Capability on Display-M.2 Adapter~~Card~~	**Example**	**DP_MLDIR Pin Termination on Display-M.2 Adapter~~Card~~**
DisplayPort Sink	Card is a wireless display transmitter	Terminated directly to GND
DisplayPort Source	Card is a wireless display receiver	Terminated directly to ~~+~~3.3 V
DisplayPort Sink or Source	Card is configurable as either a wireless display transmitter or receiver	Hi-Z (single input load)

3.1.7. SDIO Interface

The M.2 SDIO interface comprise of the following Standard SDIO signals:

- Four bi-directional Data signals, each capable of data rates up to 208 Mb/s (for a total of 832 Mb/s~~.~~)
- One bi-directional CMD signal~~.~~
- One Clock signal up to 208 MHz

These signals, supporting up to SDR104, are in accordance to standard SDIO specifications. Refer to the *SDIO3.0 Specification* for more details on the functional requirements for the SDIO interface signals.

The M.2 SDIO interface also includes two non-standard signals in support of new features related to the SDIO interface. This includes the following signals:

- **SDIO_WAKE#**
  This signal is an output from the Adapter ~~device~~ (comms Adapter~~module~~) to the ~~platform~~ Platform used to trigger the wake to the host and to initiate SDIO interface communication between the Adapter ~~device~~ and the ~~platform~~Platform. This signal is an open drain output and needs to be pulled high by a ~~platform~~ Platform resistor to 1.8 V (recommended pull up value should be between 15 kΩ to 100 kΩ).
- **SDIO_RESET#**
  This signal is an input to the Adapter ~~device~~ from the ~~platform~~ Platform and it is used to reset the SDIO interface. The signal is 1.8 V at the Adapter ~~module~~ input.

Since the SDIO_RESET# and SDIO_WAKE# are not part of the *~~standard~~ SDIO 3.0 ~~s~~Specification*, the timing diagrams shown in Figure 92 and Figure 93 show their expected timing behavior. Table 19 lists the SDIO reset and power-up timing parameters.

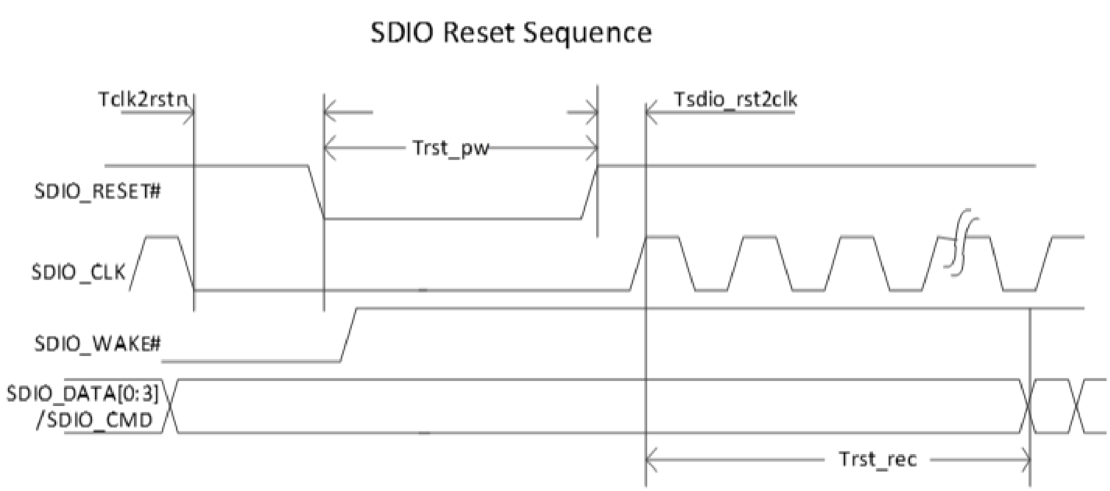


Figure 92. SDIO Reset Sequence

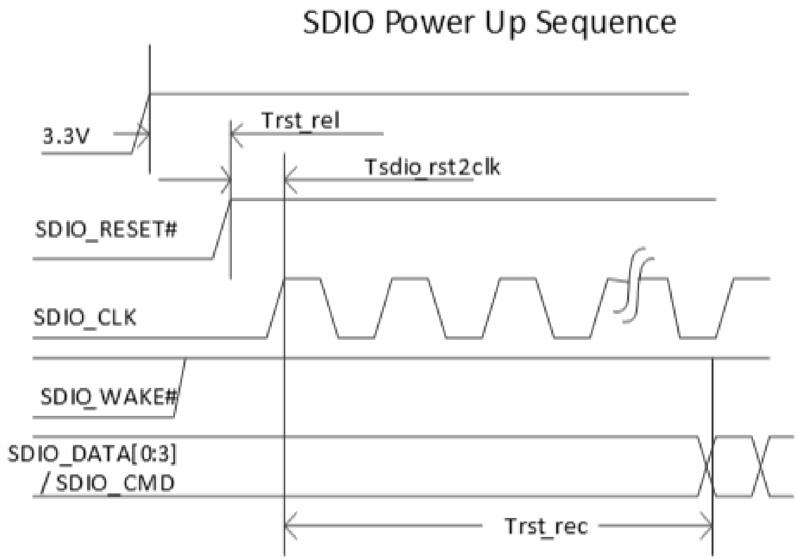


Figure 93. SDIO Power-up Sequence

Table 19. SDIO Reset and Power-up Timing

Symbol	Parameter	Min	Max	Unit
T_{rst_rel}	This time is measured from 3.3 V ≥ 2.9 V	1		µs
$T_{sdio\_rst2clk}$	10x clock cycles of 400 kHz	25		µs
T_{rst_rec}	The time needed to allow power up the DC/DC and some basic configuration operations	100		µs
$T_{clk2rstn}$		0		
T_{rst_pw}	Reset pulse width	10		µs

SDIO_WAKE# ~~can be~~is asserted by the device at any given time and it is NOT bound by timing constraint. Yet, from functionality point of view it is expected that:

- The SDIO_WAKE# will be asserted (~~“0”~~driven low) only when the host is in sleep and the device needs a service from the host.
- The SDIO_WAKE# will be asserted and will not de-assert before the source for the assertion is served in the device.

3.1.8. UART Interface

The Universal Asynchronous Receiver and Transmitter (UART) interface ~~can be~~is used for communication with other host controllers or systems.

The UART ~~can~~ handles 8-bit data frames and inserts one start and one stop bit (with/without parity). The format of the UART frame is in Figure 94.

Idle	Start	0	1	2	3	4	5	6	7	Parity	Stop	Idle

Idle	Start	0	1	2	3	4	5	6	7	Stop	Idle

Figure 94. UART Frame Format

The UART power management protocol supports the following 4-wire and 5-wire interfaces:

- UART_RXD (Input): Receive Data
- UART_TXD (Output): Transmit Data
- UART_RTS (Output): Request to Send (Host Flow Control)
- UART_CTS (Input): Clear to Send (Device Flow Control)

To enable additional power management protocols, an additional, non-standard UART interface is included:

- UART_WAKE# (Output): Host wake-up line is optional Out of Band in case the host does not support in band wake-up messaging.

3.1.8.1. UART_WAKE#

The UART_WAKE# signals is an Open Drain, Active Low signal used to Wake the Host or enable the Host to go into Sleep modes. The UART_WAKE# ~~can be~~is used as an Out of Band signal to the Host in case the host does not support in-band wake up using an In-Band message. The UART_WAKE# signal requires a pull up on the host side (recommended pull up value should be between 15 kΩ to 100 kΩ).

There are potentially many ways to make use of this Out of Band Wake signal and they ~~may be~~are VENDOR DEFINED.

3.1.9. PCM/I2S Interface

The following features are supported by the PCM interface:

- Four wire interface:
  - Clock signal
    PCM_CLK/I2S SCK: ~~;-~~Output if master, Input if slave
  - Two frame signals
    PCM_SYNC/I2S WS: ~~-~~Output if master, Input if slave
  - Data in
    PCM_IN/I2S SD_IN: Input
  - Data out signal
    PCM_OUT/I2S SD_OUT: Output
- Single bidirectional PCM channels
- 16-bit and 24-bit data words
- Various PCM data sample rates including 8 kHz and 16 kHz are supported

The PCM/I2S mode is used for Standard (Narrowband) Mono speech or Wideband Mono speech. I2S will also be used for offloading of stereo audio data from the host (A2DP offload).

The PCM interface consists of four signals as shown in Figure 95.

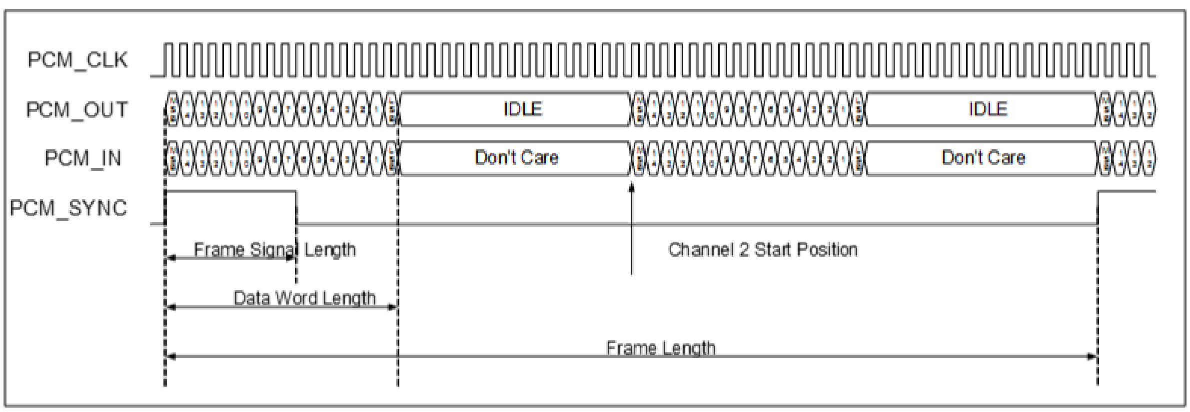


Figure 95. Typical PCM Transaction Timing Diagram

The clock signal PCM_CLK is the timing base for the other signals in the PCM interface. In clock master mode, the Bluetooth device generates PCM_CLK from the internal system clock using a fractional divider. In clock slave mode PCM_CLK is an input to the Bluetooth device and has to be supplied by an external source.

The PCM interface supports one bidirectional channel. Data is transmitted on PCM_OUT and received on PCM_IN; always with the most significant bit first. The 16-bit linear audio samples and 8-bit A-law or µ-law compressed audio samples are supported.

3.1.10. I2C Interface

3.1.10.1. Alert# Signal

This ALERT# signal is intended to indicate to the ~~platform~~Platform~~/system~~ that the I2C device requires attention. This GPIO ~~can be~~is used to establish specific communication/signaling to the host from the device. This signal is Active Low.

3.1.10.2. I2C_DATA Signal

The I2C_DATA signal is used to send the data packets from the host to the device according to the I2C protocol. The speed supported on this line depends on the host I2C_CLOCK signal speeds and the device processing capability.

3.1.10.3. I2C_CLOCK Signal

The I2C_CLOCK signal provides the clock signaling from the host to the device to be able to decode the data on the I2C_DATA line.

3.1.11. NFC Supplemental UIM Interface

The UIM POWER SRC, UIM POWER SNK, and UIM SWP signals are supplemental NFC signals that ~~can be~~are used when a UIM device is implemented as the Secure Element.

3.1.11.1. UIM~~MI~~ POWER SRC

In systems where there is a WWAN device on one M.2 ~~C~~Adapter ~~ard~~ and an NFC solution on another M.2 Adapter~~Card~~, then the WWAN UIM PWR output must be routed to the UIM POWER SRC pin of the M.2 Adapter ~~Card~~ on which the NFC device is located. This UIM power signal is basically passed through the NFC device and output through the UIM POWER SNK signal described in the following paragraphs.

3.1.11.2. UIM POWER SNK

Refer to the ISO/IEC 7816-3 for more details on the voltage and current tolerance requirements for the UIM_PWR power source. Note that the UIM grounding requirements ~~can be~~are provided by using any GND pin. Only PCI Express M.2 Adapters ~~Card add-in cards~~ that support a UIM card ~~shall~~ are permitted to connect to this pin. If the Adapter ~~add-in card~~ has UIM support capabilities, it must support the UIM_PWR power source at the appropriate voltage for each class of operating conditions (~~for example~~e.g., voltage) supported as defined in ISO/IEC 7816-3.

In this case, the UIM_POWER_SNK maps to contact number C1 as defined in ISO/IEC 7816-2.

3.1.11.3. UIM SWP

NFC includes a SWP master using ETSI TS102.613 protocol version v7.8.0, v8.1.0, v9.1.0. SWP is a full duplex, auto-clocking interface. NFC (S1) sends using V-Domain, UICC/ SE (S2) sends using I-Domain, as described in ETSI TS102.613 in chapter 8 (Physical transmission layer).

3.1.11.4. NFC Supplemental UIM Interface Wiring Example

An example wiring diagram of the Supplemental NFC signals in conjunction with the Socket 2 and UIM/SIM device connections are shown in Figure 96.

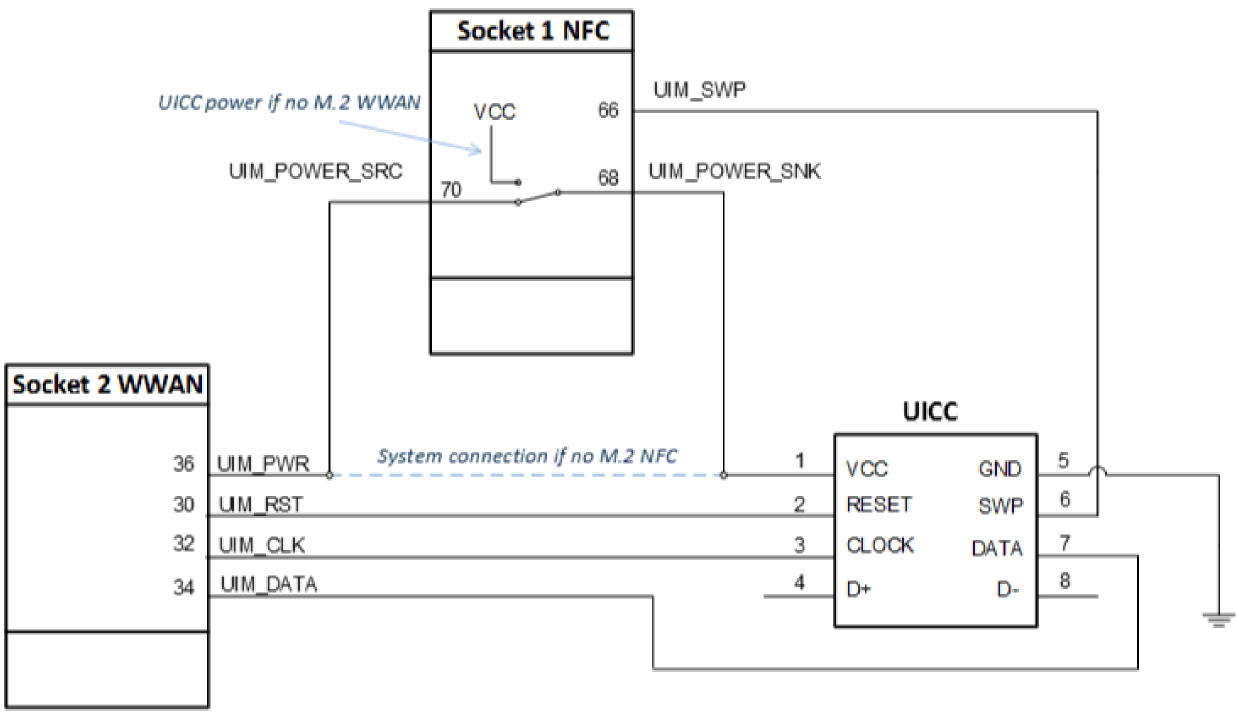


Figure 96. Supplemental NFC Signal Connection Example

3.1.12. Communication-specific Signals

3.1.12.1. Suspend Clock

The Suspend Clock (SUSCLK) is a slow clock signal running at 32.768 kHz. It is a buffered signal derived from the ~~platform~~ Platform RTC. The SUSCLK ~~Suspend Clock~~ is available during ~~platform~~ Platform normal and suspend modes of operation during which time, the Adapter ~~module can~~ makes use of this SUSCLK signal as the clock source for critical keep alive circuitry as needed. The SUSCLK is not available in ~~platform~~ Platform hard shut down modes at which point, the 3.3 V power to the Adapter ~~module~~ is also shut down. SUSCLK will have a duty cycle that ~~can be~~is permitted to be as low as 30% or as high as 70%. Accuracy will be up to 200 ppm.

3.1.12.2. Status Indicators

Two LED# signals are provided to enable wireless communication Adapter ~~add-in cards~~ to provide status indications to users via system provided indicators.

LED_1# and LED_2# output signals are active low and are intended to drive system-mounted LED indicators. These signals ~~shall~~ must be capable of sinking to ground a minimum of 9.0 mA at up to a maximum V_{OL} of 400 mV.

Figure 97 is an example of how such LEDs are typically connected in a ~~platform~~Platform~~/system~~ using 3.3 V.

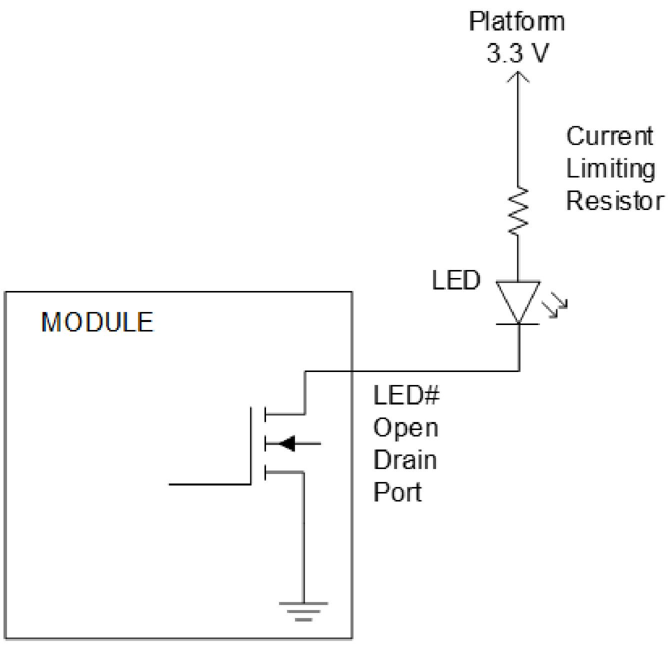


Figure 97. Typical LED Connection Example in ~~Platform~~Platform/System

In a typical LED connection case, the current limiting resistor value will be in the 100 Ω range to enable the 9 mA current needed to light up the LED when tied up to a 3.3 V rail. Other ~~platform~~ Platform LED connections are possible including other alternate voltage sources. However, caution should be used to prevent back-biasing through the LED# pin in various power states.

Table 20 presents a simple indicator protocol for each of two defined LED states as applicable for wireless radio operation. Although the actual definition of the indicator protocol is established by the OEM system developer, the interpretations ~~may be~~are useful in establishing a minimum common implementation across many ~~platforms~~Platforms.

Table 20. Simple Indicator Protocol for LED States

State	Definition	Interpretation
OFF	The LED is emitting *no* light.	Radio is incapable of transmitting. This state is indicated when the card is not powered, a wireless disable signal is asserted to disable the radio, or when the radio is disabled by software.
ON	The LED is emitting light.	Radio is capable of transmitting. The LED should remain ON even if the radio is not actually transmitting. For example, the LED remains ON during temporary radio disablements performed by the M.2 Adapter~~Card ~~ of its own volition to do scanning, switching radios/bands, power management, etc. If the card is in a state wherein it is possible that radio ~~can ~~begins transmitting without the system user performing any action, this LED should remain ON.

More advanced indicator protocols are allowed as defined by the OEM system developer. Advanced features ~~might ~~are permitted to include use of blinking or intermittent ON states which ~~can be~~are used to indicate radio operations such as scanning, associating, or data transfer activity. Also, use of blinking states might be useful in reducing LED power consumption.

3.1.12.3. W_DISABLE# Signal

W_DISABLE1# and W_DISABLE2# are wireless disable signals that are provided for wireless communications Adapters~~add-in cards~~. These signals allow users to disable, via a system-provided switch, the Adapter~~add-in card~~'s radio operation in order to meet public safety regulations or when otherwise desired. Implementation of wireless disable signals is applicable to systems and all Adapters ~~add-in cards ~~that implement radio frequency capabilities. Multiple wireless disable signals are provided to ease managing multiple radios on a single Adapter~~add-in card~~. In cases where only one wireless disable signal is implemented by the system, the W_DISABLE1# signal must be used as the preferred control for collectively disabling all radios on the Adapters~~add-in card~~. By preferring W_DISABLE1# in these cases as the control for all on Adapter ~~module ~~wireless Comms, the W_DISABLE2# ~~could potentially~~is permitted to revert back to a Reserved pin to be used for future assignment.

The wireless disable signals are active low signals that when asserted (driven low) by the system ~~shall~~ must disable radio operation. When implemented, a pull-up resistor between each wireless disable signal and ~~+~~3.3 V is required on the card and should be in the range of 100 kΩ to 200 kΩ.

The assertion and de-assertion of each wireless disable signal is asynchronous to any system clock. All transients resulting from mechanical switches need to be de-bounced by system circuitry.

When a wireless disable signal is asserted, all of the radios associated with that signal ~~shall ~~must be disabled. When a wireless disable signal is not asserted, the associated radios ~~may ~~transmit if not disabled by other means such as software. These signals ~~may be~~are permitted to be shared between multiple M.2 Cards.

In normal operation, the card should disassociate with the wireless network and cease any further operations (transmit/receive) as soon as possible after the wireless disable signal is asserted. Given that a graceful disassociation with the wireless network fails to complete in a timely manner, the M.2 Adapter ~~Card shall~~must discontinue any communications with the network and assure that its radio operation has ceased no later than 30 s following the initial assertion of the wireless disable signal. Once the disabling process is complete, the LED specific to the radio ~~shall~~ indicates the disabled condition to the user.

The card should initiate and indicate to the user the process of resuming normal operation within 1 s of de-assertion of the wireless disable signal. Due to the potential of a software disable state, the combination of both the software state and wireless disable signal assertion state must be determined before resuming normal operation. Table 21 defines this requirement as a function of wireless disable signal and the software control setting such that the radio's RF operation remains disabled unless both the hardware and software are set to enable the RF features of the card.

The system is required to assure that each wireless disable signal be in a deterministic state (asserted or de-asserted) whenever power is applied to the Adapter~~add-in~~; ~~for example~~e.g., ~~+~~3.3 V is present.

Table 21. Radio Operational States

Wireless Disable	Signal SW Control Setting*	Radio Operation
De-asserted (HIGH)	Enable Radio (see Note)	Enabled (RF operation allowed)
De-asserted (HIGH)	Disable Radio (see Note)	Disabled (no RF operation allowed)
Asserted (LOW)	Enable Radio (see Note)	Disabled (no RF operation allowed)
Asserted (LOW)	Disable Radio (see Note)	Disabled (no RF operation allowed)

Note: *This control setting is implementation-specific and represents the collective intention of the host software to manage radio operation.

W_DISABLE1# and W_DISABLE2# are wireless disable signals that are provided for legacy wireless communications Adapters~~add-in cards~~. It is anticipated that in the future the requirement for hardware wireless disable signals will be deprecated from use in favor of in-band mechanisms.

3.1.12.4. Coexistence Signals

COEX_RXD, COEX_TXD and COEX3 are provided to allow for the implementation of wireless coexistence solutions between the radio(s) on the M.2 Adapter ~~Card~~ and other off-card radio(s). These other radios ~~can be~~are either located on another M.2 Adapter ~~Card~~ located in the same host ~~platform~~ Platform or as alternate radio implementations (~~for example~~e.g., using a PCI Express Mini CEM or a proprietary form-factor add-in solution).

The COEX_RXD and COEX_TXD signals are for a UART communication path between the WWAN radio solution and the wireless solutions on the Connectivity Adapter~~module~~. The coexistence protocol of these signals is based on the BT-SIG coexistence protocol.

- COEX_TXD is the UART transmit signal from the Connectivity Adapter ~~module~~ to the WWAN solution.

- COEX_RXD is the UART receive signal from the WWAN solution to the Connectivity Adapter. ~~module~~

The pin assignment ~~can be~~is seen in the pinout diagram and coincides with the signals in the Socket 2 pinouts.

The functional definition of the COEX3 pin is OEM-specific and should be coordinated between the host ~~platform~~ Platform OEM and card vendors. The ordered labeling of these signals in this specification is intended to help establish consistent implementations, where practical, across multiple instances of cards in the host ~~platform~~Platform.

3.1.13. Reserved Pins

It is expected that the Reserved pins are not terminated on either the Adapter ~~add-in card~~ or system board-side of the connector. These pins are reserved for definition in future revisions of this specification. Non-standard use of these pins may result in incompatibilities in solutions aligned with the future revisions.

3.1.14. Vendor Defined

These pins are vendor defined and fall under the BTO/CTO definitions between vendor and customer.

3.1.15. Socket 1 Connector Pinout Definitions

> All pinouts tables in this section are written from the ~~module~~ Add-in Card point of view when referencing signal directions.

The following tables illustrate signal pinouts for the Add-in Card ~~module~~ edge card connector:

- Table 22 lists the pinout for the SDIO based solution pinouts.
- Table 23 lists the pinout for the Display Port based solution pinouts.
- Table 24 lists the pinout for a basic Add-in Card ~~module~~ solution using the common host interfaces and utilizes a Dual Add-in Card ~~Module~~ key that will enable it to plug into two socket 1 types (Keys).

There are also ~~module~~ Module pinouts definitions for Type 1216, Type 2226, and Type 3026 LGA soldered down ~~modules~~ Modules in section3.1.16, *Socket 1 Based Soldered-down Module Pinouts.*

Table 22. SDIO Based Add-in Card ~~Module~~ Solution Pinouts (~~Module~~ Key E)

Pin	Signal	Signal	Pin
		GND	75
74	3.3 V	RESERVED/REFCLKn1	73
72	3.3 V	RESERVED/REFCLKp1	71
70	UIM_POWER_SRC/GPIO_1/PEWAKE1#	GND	69
68	UIM_POWER_SNK/CLKREQ1#	RESERVED/PETn1	67
66	UIM_SWP/PERST1#	RESERVED/PETp1	65
64	RESERVED	GND	63
62	ALERT# (O)(0/1.8 V)	RESERVED/PERn1	61
60	I2C_CLK (I)(0/1.8 V)	RESERVED/PERp1	59
58	I2C_DATA (I/O)(0/1.8 V)	GND	57
56	W_DISABLE1# (I)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
54	W_DISABLE2# (I)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
52	PERST0# (I)(0/3.3V)	GND	51
50	SUSCLK(32kHz) (I)(0/3.3V)	REFCLKn0	49
48	COEX_RXD (I)(0/1.8V)	REFCLKp0	47
46	COEX_TXD (O)(0/1.8V)	GND	45
44	COEX3 (I/O)(0/1.8V)	PETn0	43
42	VENDOR DEFINED	PETp0	41
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PERn0	37
36	UART CTS (I)(0/1.8V)	PERp0	35
34	UART RTS (O)(0/1.8V)	GND	33
32	UART RXD (I)(0/1.8V)	ADD-IN CARD ~~Module~~ KEY E	
	ADD-IN CARD ~~Module~~ KEY E	ADD-IN CARD ~~Module~~ KEY E	
	ADD-IN CARD ~~Module~~ KEY E	ADD-IN CARD ~~Module~~ KEY E	
	ADD-IN CARD ~~Module~~ KEY E	ADD-IN CARD ~~Module~~ KEY E	
	ADD-IN CARD ~~Module~~ KEY E	SDIO RESET#/Tx_BLANKING (I)(0/1.8V)	23
22	UART TXD (O)(0/1.8V)	SDIO WAKE# (O)(0/1.8V)	21
20	UART WAKE# (O)(0/3.3V)	SDIO DATA3 (I/O)(0/1.8V)	19
18	GND	SDIO DATA2 (I/O)(0/1.8V)	17
16	LED_2# (O)(OD)	SDIO DATA1 (I/O)(0/1.8V)	15
14	PCM_IN/I2S SD_IN (I)(0/1.8V)	SDIO DATA0 (I/O)(0/1.8V)	13
12	PCM_OUT/I2S SD_OUT (O)(0/1.8V)	SDIO CMD (I/O)(0/1.8V)	11
10	PCM_SYNC/I2S WS (I/O)(0/1.8V)	SDIO CLK/SYSCLK (I)(0/1.8V)	9
8	PCM_CLK/I2S SCK (I/O)(0/1.8V)	GND	7
6	LED_1# (O)(OD)	USB_D-	5
4	3.3 V	USB_D+	3
2	3.3 V	GND	1

Table 23. Display Port Based Add-in Card ~~Module~~ Solution Pinouts (~~Module~~ Key A)

Pin	Signal	Signal	Pin
		GND	75
74	3.3 V	REFCLKn1	73
72	3.3 V	REFCLKp1	71
70	PEWAKE1# (I/O)(0/3.3V)	GND	69
68	CLKREQ1# (I/O)(0/3.3V)	PETn1	67
66	PERST1# (I)(0/3.3V	PETp1	65
64	RESERVED	GND	63
62	ALERT# (O)(0/1.8V)	PERn1	61
60	I2C_CLK (I)(0/1.8V)	PERp1	59
58	I2C_DATA (I/O)(0/1.8V)	GND	57
56	W_DISABLE1# (I)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
54	W_DISABLE2# (I)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
52	PERST0# (I)(0/3.3V)	GND	51
50	SUSCLK(32kHz) (I)(0/3.3V)	REFCLKn0	49
48	COEX_RXD (I)(0/1.8V)	REFCLKp0	47
46	COEX_TXD (O)(0/1.8V)	GND	45
44	COEX3 (I/O)(0/1.8V)	PETn0	43
42	VENDOR DEFINED	PETp0	41
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PERn0	37
36	GND	PERp0	35
34	DP_ML0p	GND	33
32	DP_ML0n	DP_HPD (I/O)(0/3.3V)	31
30	GND	GND	29
28	DP_ML1p	DP_ML2p	27
26	DP_ML1n	DP_ML2n	25
24	GND	GND	23
22	DP_AUXp	DP_ML3p	21
20	DP_AUXn	DL_ML3n	19
18	GND	DP_MLDIR GND (In)/ 3.3V (Out)/NC (I/O)	17
16	LED_2# (O)(OD)	ADD-IN CARD ~~Module~~ KEY A	
	ADD-IN CARD ~~Module~~ KEY A	ADD-IN CARD ~~Module~~ KEY A	
	ADD-IN CARD ~~Module~~ KEY A	ADD-IN CARD ~~Module~~ KEY A	
	ADD-IN CARD ~~Module~~ KEY A	ADD-IN CARD ~~Module~~ KEY A	
	ADD-IN CARD ~~Module~~ KEYA A	GND	7
6	LED_1# (O)(OD)	USB_D-	5
4	3.3 V	UDB_D+	3
2	3.3 V	GND	1

Table 24. Socket 1 ~~Module~~ Add-in Card Pinouts (~~Module~~ Key A-E)

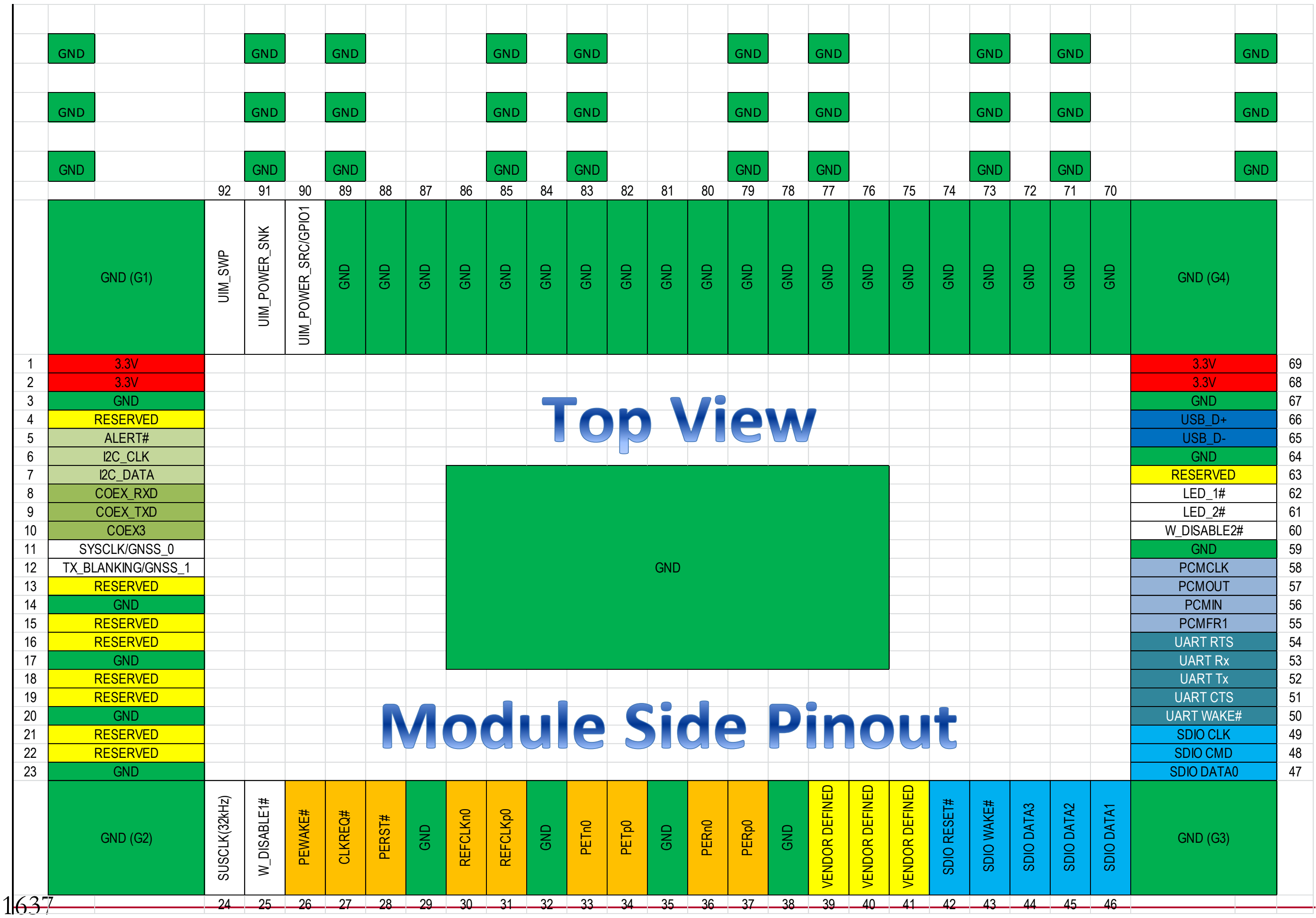
Pin	Signal	Signal	Pin
		GND	75
74	3.3 V	RESERVED/REFCLKn1	73
72	3.3 V	RESERVED/REFCLKp1	71
70	UIM_POWER_SRC/GPIO_1/PEWAKE1#	GND	69
68	UIM_POWER_SNK/CLKREQ1#	RESERVED/PETn1	67
66	UIM_SWP/PERST1#	RESERVED/PETp1	65
64	RESERVED	GND	63
62	ALERT# (O)(0/1.8 V)	RESERVED/PERn1	61
60	I2C_CLK (I)(0/1.8 V)	RESERVED/PERp1	59
58	I2C_DATA (I/O)(0/1.8 V)	GND	57
56	W_DISABLE1# (I)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
54	W_DISABLE2# (I)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
52	PERST0# (I)(0/3.3V)	GND	51
50	SUSCLK(32kHz) (I)(0/3.3V)	REFCLKn0	49
48	COEX_RXD (I)(0/1.8V)	REFCLKp0	47
46	COEX_TXD (O)(0/1.8V)	GND	45
44	COEX3(I/O)(0/1.8V)	PETn0	43
42	VENDOR DEFINED	PETp0	41
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PERn0	37
36	NC	PERp0	35
34	NC	GND	33
32	NC		
	~~Module~~ ADD-IN CARD KEY E	ADD-IN CARD ~~Module~~ KEY E	
	ADD-IN CARD ~~Module~~ KEY E	ADD-IN CARD ~~Module~~ KEY E	
	ADD-IN CARD ~~Module~~ KEY E	ADD-IN CARD ~~Module~~ KEY E	
	ADD-IN CARD ~~Module~~ KEY E	ADD-IN CARD ~~Module~~ KEY E	
22	NC	NC	23
20	NC	NC	21
18	GND	NC	19
16	LED_2# (O)(OD)	NC	17
	ADD-IN CARD ~~Module~~ KEY A	ADD-IN CARD ~~Module~~ KEY A	
	ADD-IN CARD ~~Module~~ KEY A	ADD-IN CARD ~~Module~~ KEY A	
	ADD-IN CARD ~~Module~~ KEY A	ADD-IN CARD ~~Module~~ KEY A	
	ADD-IN CARD ~~Module~~ KEY A	ADD-IN CARD ~~Module~~ KEY A	
6	LED_1# (O)(OD)	GND	7
4	3.3 V	USB_D-	5
2	3.3 V	USB_D+	3
		GND	1

3.1.16. Socket 1 Based Soldered-down Module Pinouts

> All pinouts tables in this section are written from the ~~module~~ Module point of view when referencing signal directions.

This section contains the ~~module~~ Module pinouts maps for Type 2226, Type 1216, and Type 3026 LGA soldered-down ~~modules~~Modules:

- Figure 98 shows the Type 2226 SDIO Based Module-side Pinout
- Figure 99 shows the Type 1216 SDIO Based Module-side Pinout
- Figure 100 shows the Type 3026 Display Port Pinouts Extension Over an SDIO Based Module-side Pinout


Top View
Module Side Pinout
GND
GND (G1)
GND (G2)
GND (G3)
GND (G4)
92 UIM_SWP
91 UIM_POWER_SNK
90 UIM_POWER_SRC/GPIO1
89 GND
88 GND
87 GND
86 GND
85 GND
84 GND
83 GND
82 GND
81 GND
80 GND
79 GND
78 GND
77 GND
76 GND
75 GND
74 GND
73 GND
72 GND
71 GND
70 GND
1 3.3V
2 3.3V
3 GND
4 RESERVED
5 ALERT#
6 I2C_CLK
7 I2C_DATA
8 COEX_RXD
9 COEX_TXD
10 COEX3
11 SYSCLK/GNSS_0
12 TX_BLANKING/GNSS_1
13 RESERVED
14 GND
15 RESERVED
16 RESERVED
17 GND
18 RESERVED
19 RESERVED
20 GND
21 RESERVED
22 RESERVED
23 GND
3.3V 69
3.3V 68
GND 67
USB_D+ 66
USB_D- 65
GND 64
RESERVED 63
LED_1# 62
LED_2# 61
W_DISABLE2# 60
GND 59
PCMCLK 58
PCMOUT 57
PCMIN 56
PCMFR1 55
UART RTS 54
UART Rx 53
UART Tx 52
UART CTS 51
UART WAKE# 50
SDIO CLK 49
SDIO CMD 48
SDIO DATA0 47
24 SUSCLK(32kHz)
25 W_DISABLE1#
26 PEWAKE#
27 CLKREQ#
28 PERST#
29 GND
30 REFCLKn0
31 REFCLKp0
32 GND
33 PETn0
34 PETp0
35 GND
36 PERn0
37 PERp0
38 GND
39 VENDOR DEFINED
40 VENDOR DEFINED
41 VENDOR DEFINED
42 SDIO RESET#
43 SDIO WAKE#
44 SDIO DATA3
45 SDIO DATA2
46 SDIO DATA1

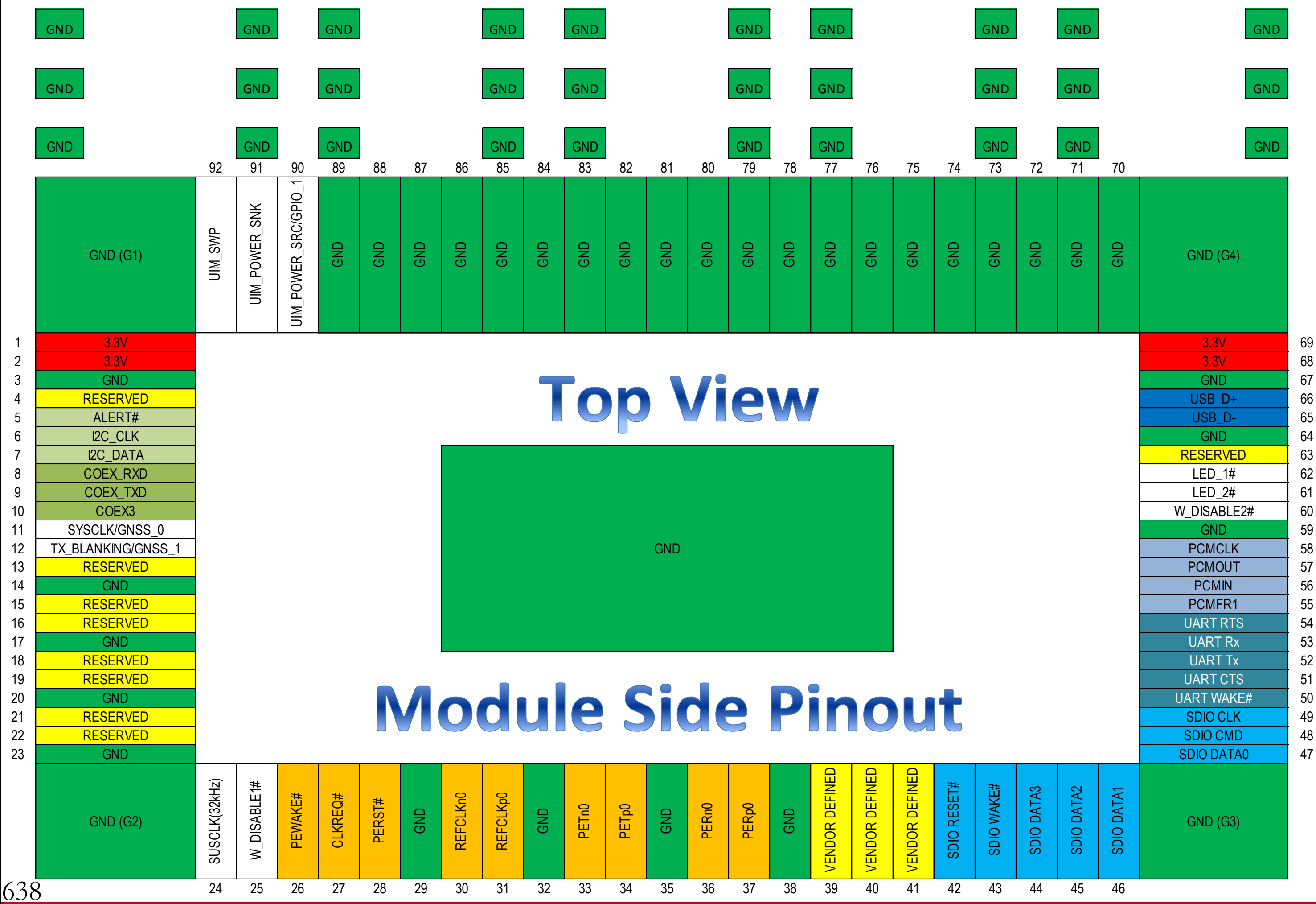
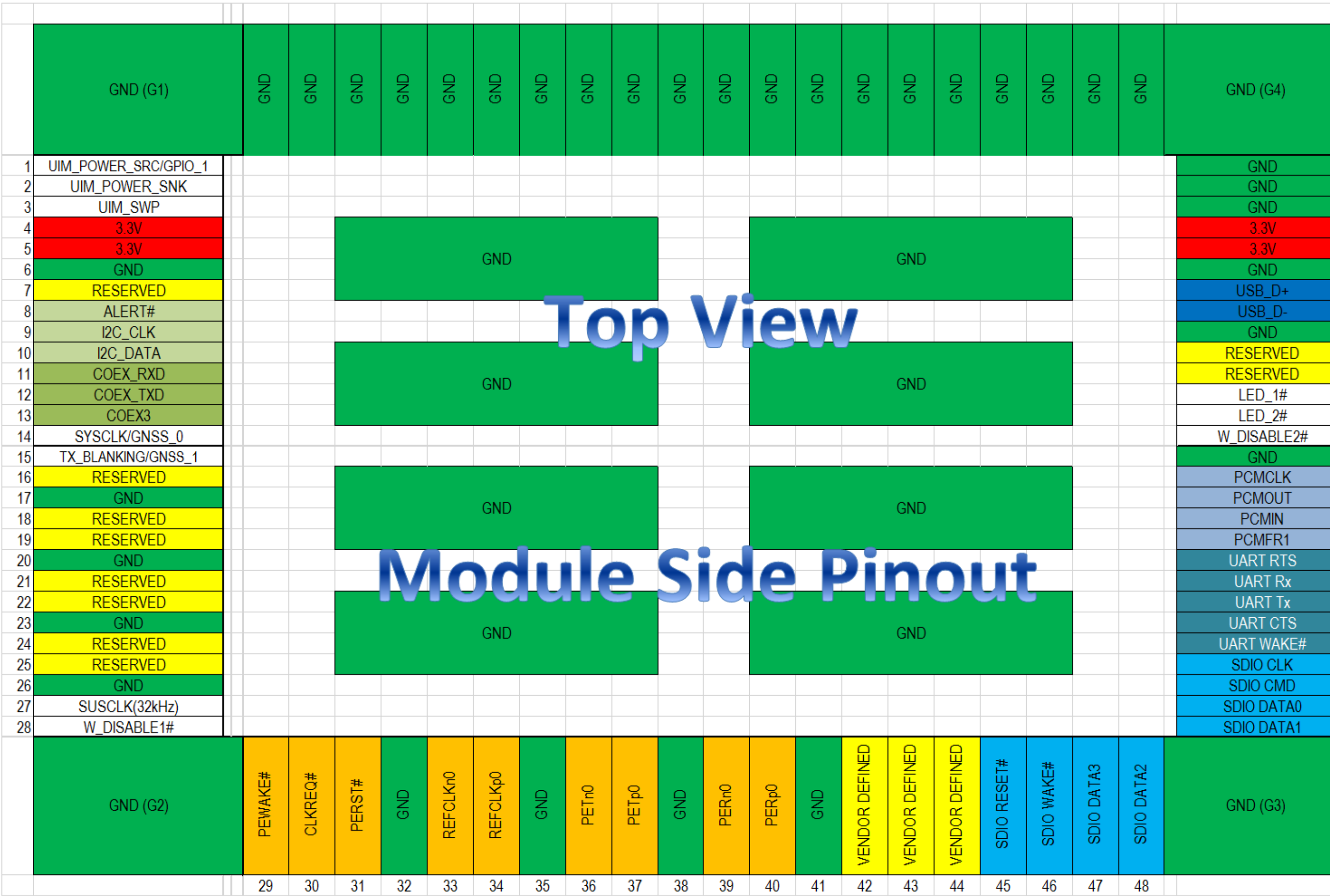


Figure 98. Type 2226 SDIO Based Module-side Pinout


Top View
Module Side Pinout
GND (G1)
GND (G4)
GND (G2)
GND (G3)
GND
1 UIM_POWER_SRC/GPIO_1
2 UIM_POWER_SNK
3 UIM_SWP
4 3.3V
5 3.3V
6 GND
7 RESERVED
8 ALERT#
9 I2C_CLK
10 I2C_DATA
11 COEX_RXD
12 COEX_TXD
13 COEX3
14 SYSCLK/GNSS_0
15 TX_BLANKING/GNSS_1
16 RESERVED
17 GND
18 RESERVED
19 RESERVED
20 GND
21 RESERVED
22 RESERVED
23 GND
24 RESERVED
25 RESERVED
26 GND
27 SUSCLK(32kHz)
28 W_DISABLE1#
GND
GND
GND
3.3V
3.3V
GND
USB_D+
USB_D-
GND
RESERVED
RESERVED
LED_1#
LED_2#
W_DISABLE2#
GND
PCMCLK
PCMOUT
PCMIN
PCMFR1
UART RTS
UART Rx
UART Tx
UART CTS
UART WAKE#
SDIO CLK
SDIO CMD
SDIO DATA0
SDIO DATA1
PEWAKE# 29
CLKREQ# 30
PERST# 31
GND 32
REFCLKn0 33
REFCLKp0 34
GND 35
PETn0 36
PETp0 37
GND 38
PERn0 39
PERp0 40
GND 41
VENDOR DEFINED 42
VENDOR DEFINED 43
VENDOR DEFINED 44
SDIO RESET# 45
SDIO WAKE# 46
SDIO DATA3 47
SDIO DATA2 48

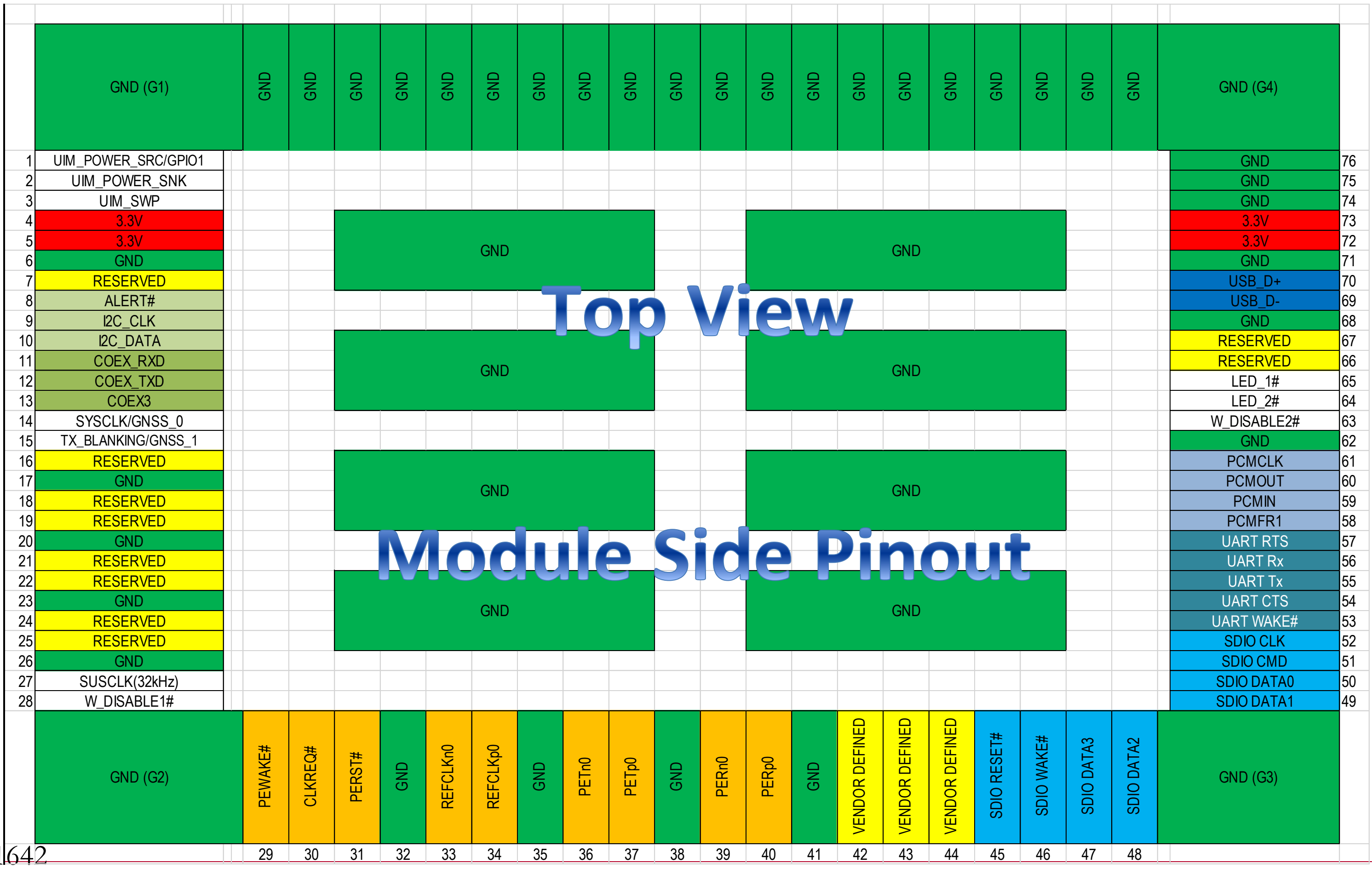
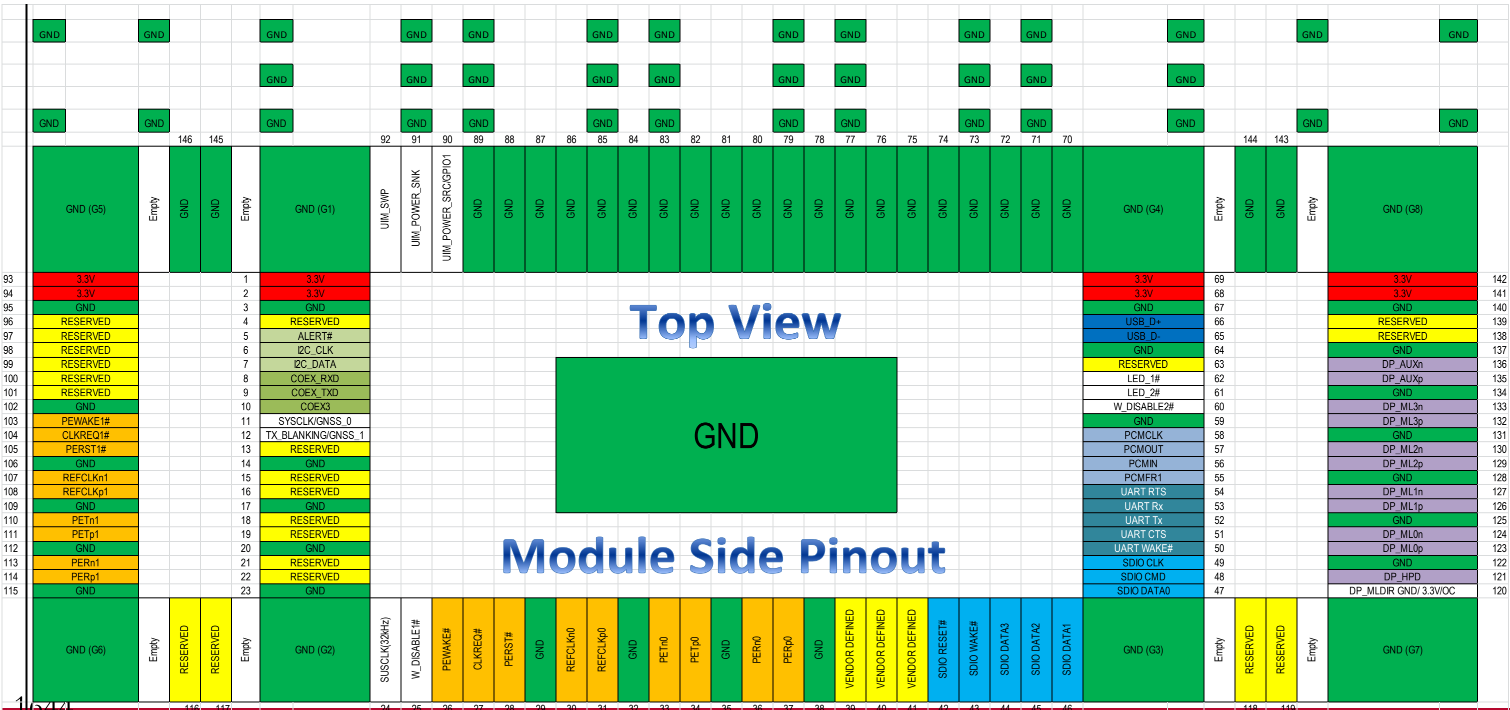


Figure 99. Type 1216 SDIO Based Module-side Pinout



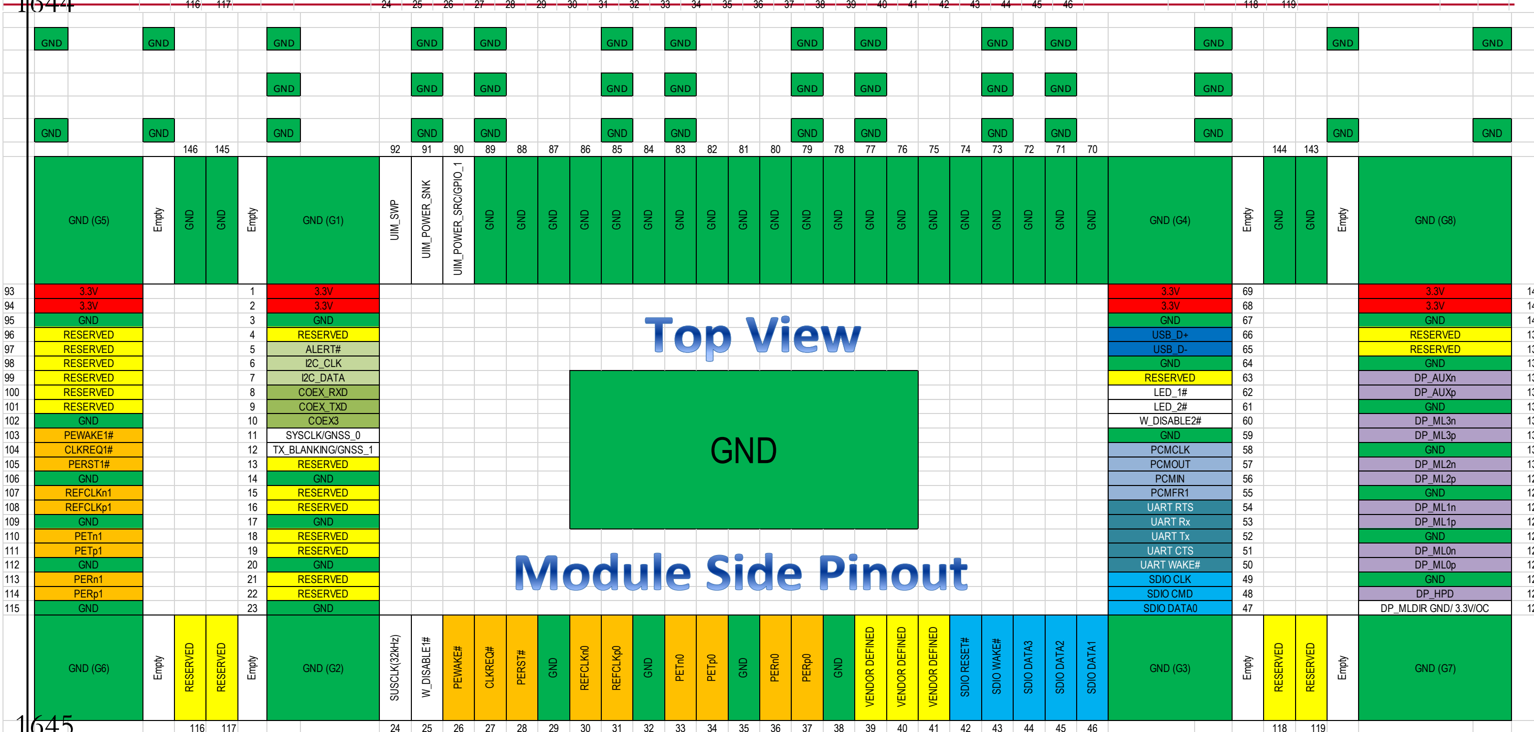


Figure 100. Type 3026 Display Port Pinouts Extension Over an SDIO Based Module-side Pinout

In this LGA pattern, the unique pins for Display Port are located on the two outer columns of the pads while the center pinouts pattern is the exact same pinouts of Type 2226. This is done so that a

land pattern footprint suitable for Type 3026 on the ~~platform~~ Platform ~~motherboard can~~ also accommodates the regular ~~Type~~ Type 2226 as an alternate option (a drop in replacement).

3.2. WWAN/SSD/Other Socket 2 ~~Module~~ Adapter Interface Signals

~~3.2.~~

The socket 2 ~~module~~ Adapter interface signals are listed in Table 25~~Table 25~~.

Table 25. Socket 2 System Interface Signal Table

Interface	Signal Name	I/O	Function	Voltage
Power and Ground	~~+~~3.3 V (5 pins)	I	3.3 V source.	3.3 V
	VIO 1.8 V	I	1.8 V I/O source (low current)	1.8 V
	GND (11 pins)		Return current path.	0 V
Communication-specific Signals	SUSCLK	I	32.768 kHz clock supply input that is provided by the ~~platform~~ Platform chipset to reduce power and cost for the ~~module~~Adapter. SUSCLK duty cycle is permitted to be as low as 30% or as high as 70%. The tolerance for this clock is ±100 ppm~~SUSCLK will have a duty cycle that can be as low as 30% or as high as 70%. 200 ppm~~.	3.3 V
	W_DISABLE1#	I	Active low, debounced signal when applied by the system it will disable radio operation on the ~~add-in cards~~Adapters that implement radio frequency applications. When implemented, these signals require a pull-up resistor on the card.	3.3 V
	W_DISABLE2#	I		1.8 V
	LED_1#~~[1]~~ (see Note 1)	O	Open drain, active low signal. These signals are used to allow the ~~add-in card~~Adapters to provide status indicators via LED devices that will be provided by the system.	3.3 V
	COEX_RXD COEX_TXD COEX3	I O I/O	Coexistence between WWAN and WiFi+BT on Socket 1. UART TxD and RxD signals per BT-SIG coexistence protocol + an undefined signal.	1.8 V
Supplemental Communication-Specific Signals	FULL_CARD_POWER_OFF#	I	A single control to turn Off the WWAN solution. It is Active Low. This is only required on Tablet devices working directly off V_{BAT}.	1.8 V Nominal /3.465 V Max
	RESET#	I	A single control to Reset the WWAN solution. Active Low. This is needed when working in ~~systems/platform~~Platforms running directly off V_{BAT}.	1.8 V

~~1 LED_1# is valid for SSDs as well.~~

Interface	Signal Name	I/O	Function	Voltage
	GPIO_[0..11]~~0F~~ (See Note 2)[2]	I/O	These signals form a block of programmable signals which ~~can be~~are used to perform various functions. See Table 26 for specific functions performed.	1.8 V
Supplemental Communication-specific Signals **continued…**	ANTCTL[0..3]	I/O	These signals are used for Antenna Control. Two modes of operation are supported: GPIO and RFFE (see 3.2.11.5, Antenna Control).	1.8 V Nominal / 2.8 V Max
	IPC_[0..7]	I/O	Pins to facilitate IPC signals exchanged between the host and the card. Functions are BTO/CTO.	1.8 V
	AUDIO[0..3]	I/O	Pins for the use of audio. Two modes are supported: I2S and SLIMBus (see S~~s~~ection 3.2.11.3.2~~, Audio Signals~~).	1.8 V
	WAKE_ON_WWAN#	O	Used to wake the ~~platform~~ Platform by the WWAN device.	1.8 V
	DPR	I	This signal is an input directly to the WWAN ~~module~~ Adapter from a suitable SAR sensor. The specific implementation will be determined by the ~~module~~ Adapter vendor and their customer.	1.8 V
PCI-e	PERp0, PERn0/ PETp0, PETn0 PERp1, PERn1/ PETp1, PETn1	I/O	PCIe TX/RX Differential signals defined by the *PCI Express CEM Specification*.	
	REFCLKp/ REFCLKn	I	PCIe Reference Clock signals (100 MHz) defined by the *PCI Express CEM Specification*.	
	PERST#	I	PCIe -Reset is a functional reset to the card as defined by the *PCI Express ~~PCIe~~ Mini CEM Specification*.	3.3 V (Note 3)[3] 1.8 V (Note 4)[4]
	CLKREQ#	I/O	Clock Request is a reference clock request signal as defined by the *PCI Express Mini CEM Specification*.~~PCIe Mini CEM specification.~~ Open Drain with pull up on ~~platform~~Platform. Active Low; also used by L1 PM Substates.	3.3 ~~V~~[3]V (Note 3) 1.8 V [4](Note 4)
	PEWAKE#/OBFF	I/O	PCIe WAKE#. Open Drain with pull up on ~~platform~~Platform. Active Low when used as PEWAKE#. When the ~~add-in module~~Adapter supports wakeup, this signal is used to request that the system return from a sleep/suspend	3.3 V (Note 3) 1.8 V (Note 4)~~3.3 V~~[3] ~~1.8 V~~[4]

[2] ~~GPIO_[9] may be defined as LED_1#, IPC_7, or SATA DAS/DSS#. Host systems should use the CONFIG pins (see 3.2.12), or other mechanisms, to ensure that these signals are fully electrically compatible, or that no electrically incompatible signals are driven onto these pins of an M.2 module~~ Adapter ~~prior to discovery of the module~~ Adapter ~~type~~.~~,~~

[3] ~~Key B~~

[4] ~~Key C~~

Interface	Signal Name	I/O	Function	Voltage
			state to service a function initiated wake event. When the Adapter ~~add-in module~~ supports OBFF mechanism, the signal is used by the system to indicate OBFF or CPU Active State transitions.	
M-PCIe	MPERp0, MPERn0/ MPETp0, MPETn0	I/O	M-PCIe TX/RX Differential Signals defined by the *PCI Express Base Specification*.	
	MREFCLKp/MREFCLKn	I	M-PCIe Reference Clock Signals defined by the *PCI Express Base Specification.*	
USB	USB D+, USB D-	I/O	USB Data ± Differential defined in the *USB 2.0 Specification*.	
USB3.1 Gen1	USB3.1-Rx+ USB3.1-Rx- USB3.1-Tx+ USB3.1-Tx-	I/O	USB3.1 Gen1 TX/RX Differential signals defined by the *USB3.1 ~~s~~Specification*.	
HSIC	HSIC-DATA, HSIC-STROBE	I/O	HSIC Data and Strobe signals as functionally defined by the *HSIC Electrical Specification*.	1.2 V
SSIC	SSIC-RxP, SSIC-RxN SSIC-TxP, SSIC-TxN	I/O	SSIC Tx/Rx Differential signals defined in the *SSIC S~~s~~pecification*.	
SATA	SATA-A+, SATA-A-/ SATA-B+, SATA-B-	I/O	Refer to the *Serial ATA Specification.*	
	DEVSLP	I		
	DAS/DSS#	I/O		
SSD Specific Signals	Reserved for MFG_DATA/Reserved for MFG_CLOCK		Dedicated Data and Clock pins for SSD Manufacturing. Not to be connected to in the ~~platform~~ Platform system.	
	ALERT#	O	Alert notification to master; Open Drain with pull-up on ~~platform~~Platform; Active low.	1.8 V
	SMB_CLK	I/O	SMBus Clock; Open Drain with pull-up on ~~platform~~Platform.	1.8 V
	SMB_DATA	I/O	SMBus Data; Open Drain with pull-up on ~~platform~~Platform.	1.8 V
User Identity Module (UIM) Signals	SIM_DETECT	I	This is an indication to the modem to detect the SIM insertion/removal. It is usually connected to the SIM reader SW pin and is card type dependent.	1.8 V
	UIM_RESET	O	UIM reset signal. Compliant to the *ISO/IEC 7816-3 specification (RST)*.	
	UIM_PWR	O	Power source for the UIM. Compliant to the *ISO/IEC 7816-3 Specification (VCC)*.	
	UIM_CLK	O	UIM clock signal. Compliant to the *ISO/IEC 7816-3 Specification (CLK).*	

Interface	Signal Name	I/O	Function	Voltage
	UIM_DATA	I/O	UIM data signal. Compliant to the *ISO/IEC 7816-3 specification (I/O).*	
~~Module~~ Add-in Card Configuration Pins	CONFIG_0..3	O	These signals provide the means to indicate the specific configuration of the Add-in Card ~~module~~ as well as indication of whether an Add-in Card ~~module~~ is present or not. The meaning of each of the 16 possible decodes is shown in Table 29. These signals should either be grounded or left No Connect to build the decode required for a given Add-in Card ~~module~~ type. The host must provide a pull up resistor for each of these signals to either 1.8 V or 3.3 V.	0 V (GND) or ~~/~~NC
Modular Vendor Defined Pins	VENDOR_PORT_(A, B, C)	I/O	These signals are Vendor defined. Example definitions ~~can be~~are ~~found~~ shown in the Annex ~~Annex~~ section.	

Notes:

1. LED_1# is valid for SSDs as well.
2. GPIO_9 may be defined as LED_1#, IPC_7, or SATA DAS/DSS. Host systems should use the CONFIG pins (see 3.2.12), or other mechanisms, to ensure that these signals are fully electrically compatible, or that no electrically incompatible signals are driven onto these pins of an M.2 Adapter prior to discovery of the Adapter type.
3. Key B
4. Key C

3.2.1. Power Sources and Grounds

~~3.2.1. Power Sources and Grounds~~

PCI Express M.2 Socket 2 utilizes a single power sources (3.3 V) to power main circuitry on the ~~module~~ Adapter similar to that of Socket 1. The voltage source (~~+~~3.3 V) is expected to be available during the system's stand-by/suspend state to support wake event processing on the communications card. In socket 2, there is provision for five 3.3 V pins to enable higher continuous current if required.

Some of the higher frequency signals require additional isolation from surrounding signals using the concept of interleaving ~~ground (~~GND~~)~~ pins separating signals within the connector. These pins should be treated as a normal ground pin with connections immediately made to the ~~ground~~ GND planes within a card design.

A low current consumption 1.8 V supply pin called VIO1.8V is used to supply the on-~~module~~ Adapter I/O buffer circuitry operating at 1.8 V. ~~System platform~~Platforms that make use of pinouts that include VIO1.8V must bring this source voltage to the relevant pin in the socket connector.

3.2.2. PCI Express Interface

The PCI Express interface supported in Socket 2 is a two Lane interface intended for either WWAN, SSD, or other devices that need this sort of host interface. See S~~s~~ections 3.1.2 a~~, *PCI Express Interface*~~ ~~a~~nd 3.1.3~~, *PCI Express Auxiliary Signals* in this specification~~ for more information.

3.2.3. M-PCIe

M-PCIe combines the protocols of PCI Express with the physical layer based on the MIPI® Alliance M-PHY.

3.2.4. USB Interface

See Section 3.1.5, *USB Interface,* for a detailed description of the USB signals.

3.2.5. HSIC Interface

High-Speed Inter-Chip USB (HSIC) is a low power, chip-to-chip interconnect which is 100% host driver compatible with traditional USB cable-connected topologies. HSIC is a 2-signal (HSIC_STROBE, HSIC_DATA) serial interface which only supports the USB High-Speed 480 Mbps data rate. HSIC may be used through a connectorized interface taking into consideration the electrical limitations identified by the HSIC standard:

- Data/strobe trace length (TL) < 10 cm
- Data/strobe trace propagation skew (TS) < 15 ps

The current version of the HSIC specification is available at: http://www.usb.org/developers/docs/

3.2.6. SSIC Interface

SuperSpeed USB Inter-Chip (SSIC) is a chip-to-chip interconnect interface defined as a supplement to the *USB 3.0 Specification*. SSIC augments USB 3.0 in that the physical layer of the interconnect is based on the MIPI® Alliance M-PHY rather than the external cable-capable PHY of traditional SuperSpeed USB. This method better optimizes power, cost, and EMI robustness appropriate for being used for embedded inter-chip interfaces. All higher-layer aspects (software, transaction protocol, etc.) of SSIC follow the *USB 3.0 ~~s~~Specification*.

SSIC – Inter-Chip Supplement to the *USB 3.0 Specification*, Revision 1.0 as of May 3, 2012; available from http://www.usb.org/developers/docs/ and located within the *USB 3.0 Specification* download package.

3.2.7. USB3.1 Gen1 Interface

The USB3.1 interface supported on the M.2 connector is USB3.1 Gen1, 5 Gbps (refer to the *USB3.1 Specification*). This specification currently does not support USB3.1 Gen2, 10 Gbps. The *USB3.1 Specification* defines all electrical characteristics, enumeration, protocol, and management features to support USB3.1 Gen1 (SuperSpeed).

The SuperSpeed differential transmit lines (SSTX+, SSTX-) are required to implement the transmit path of a USB3.1 Gen1 SuperSpeed interface. These pins ~~shall be~~are connected to the transmitter differential pair in the system and to the receiver differential pair on the ~~module~~Adapter.

Likewise, SuperSpeed differential receive lines (SSRX+, SSRX-) are required to implement the receive path of a USB3.1 Gen1 SuperSpeed interface. These pins ~~shall be~~are connected to the receiver differential pair in the system and to the transmitter differential pair on the ~~module~~Adapter.

3.2.8. SATA Interface (Informative)

SATA is a high-speed serialized ATA data link interface (specifying Phy, Link, Transport, and Application layers) for hard and solid state drives as defined by the *Serial ATA International Organization* (refer to the *Serial ATA Specification*).

3.2.8.1. DEVSLP

The Device Sleep (DEVSLP)~~ (Device Sleep)~~ pin is used to inform a SATA device that it should enter the DEVSLP ~~DevSleep~~ Interface Power state (refer to the *Serial ATA Specification*).

3.2.8.2. DAS/DSS#

The Drive Activity Signal (DAS)~~ (Drive activity Signal)~~ is driven by a SATA device to indicate that an access is occurring. Hosts ~~may also~~ use the same signal for Disable Staggered Spin-up (DSS)~~ (Disable Staggered Spin-up)~~ and other functions (refer to the *Serial ATA Specification*).

3.2.9. User Identity Module (UIM) Interface

The UIM interface signals are defined on the system connector to provide the interface between the UIM and an M.2 ~~add-in card~~Adapter (e.g.,~~x.~~ WWAN, NFC). The UIM contains parameters necessary for the WWAN device's operation in a wireless wide area network radio environment. The UIM signals are described in the following paragraphs for M.2 ~~add-in cards~~Adapters that support the off-card UIM interface.

Up to two instances of UIM are permitted on an M.2 Add-in Card~~There may be up to two instances of UIM on an M.2 add-in card~~.

3.2.9.1. UIM_PWR

Refer to ISO/IEC 7816-3 for more details on the voltage and current tolerance requirements for the UIM_PWR power source. Note that the UIM grounding requirements ~~can be~~are provided by using any GND pin. Only M.2 Adapters ~~add-in cards~~ that support a UIM card ~~shall~~ are permitted to connect to this pin. If the Adapter ~~add-in card~~ has UIM support capabilities, it must support the UIM_PWR power source at the appropriate voltage for each class of operating conditions (~~for example~~e.g., voltage) supported as defined in *ISO/IEC 7816-3*. UIM_PWR maps to contact number C1 as defined in *ISO/IEC 7816-2*.

3.2.9.2. UIM_RESET

The UIM_RESET signal provides the UIM card with the reset signal. Refer to *ISO/IEC 7816-3* for more details on the functional and tolerance requirements for the UIM_RESET signal. Only M.2 ~~add~~Add-in ~~cards~~ Cards that support a UIM card ~~shall~~ are permitted to connect to this pin.

UIM_RESET maps to contact number C2 as defined in *ISO/IEC 7816-2*.

3.2.9.3. UIM_CLK

This signal provides the UIM card with the clock signal. Refer to *ISO/IEC 7816*-3 for more details on the functional and tolerance requirements for the UIM_CLK signal. Only M.2 Adapters ~~add-in cards~~ that support a UIM card ~~shall~~ are permitted to connect to this pin.

UIM_CLK maps to contact number C3 as defined in *ISO/IEC 7816-2*.

3.2.9.4. UIM_DATA

This signal is used as output (UIM reception mode) or input (UIM transmission mode) for serial data. Refer to *ISO/IEC 7816-3* for more details on the functional and tolerance requirements for the UIM_DATA signal. Only M.2 Adapters ~~add-in cards~~ that support a UIM card ~~shall~~ are permitted to connect to this pin.

UIM_DATA maps to contact number C7 as defined in *ISO/IEC 7816-2*.

3.2.9.5. SIM_DETECT

This signal is used to detect the insertion and removal of a SIM device in the SIM socket. With a Normal Short SIM Card connector, PUSH-PUSH type, the detect switch is normally shorted to ~~ground~~ GND when no SIM card is inserted. When the SIM is inserted, the SIM_DETECT will transition from a logic 0 to a logic 1 state. The rising edge will indicate insertion of the SIM card. When the SIM is pulled out, the SIM_DETECT will transition from the logic 1 to a logic 0.

This falling edge will indicate the pulling out of the SIM card. The M.2 Adapter ~~module~~ monitoring this signal will treat the rising/falling edge or the actual logic state as an interrupt, that when triggered, the Adapter ~~module~~ will act accordingly.

This will require a weak pull-up on the Adapter ~~module~~ tied to its 1.8 V power rail.

An example of a typical implementation ~~can be seen~~is shown in Figure 101.

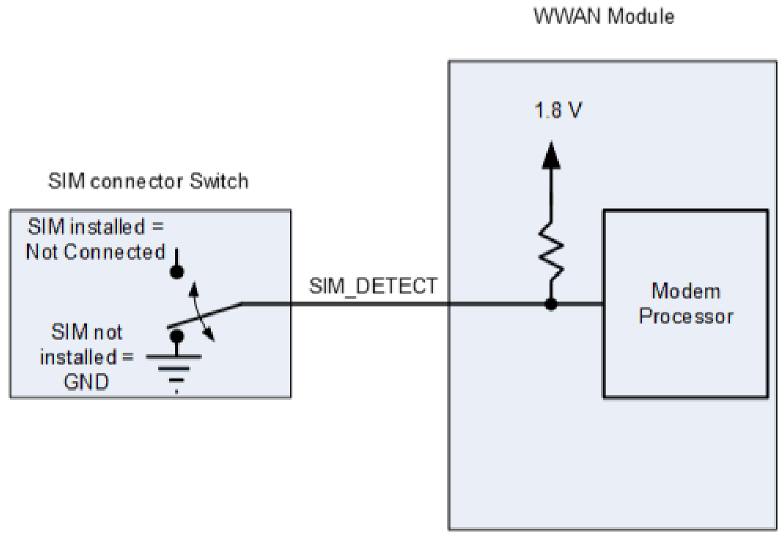


Figure 101. Typical SIM Detect Circuit Implementation

3.2.10. Communication-specific Signals

3.2.10.1. Suspend Clock

See section 3.1.12.1, *Suspend Clock* for a more detailed description of the SUSCLK signal.

3.2.10.2. Status Indicators

See section 3.1.12.2, *Status Indicators*, for a more detailed description of the LED_1# signal.

3.2.10.3. W_DISABLE# Signals

See section 3.1.12.3, *W_DISABLE# Signal* for a more detailed description of the W_DISABLE1# and W_DISABLE2# signals. It should be noted that this W_DISABLE2# of Socket 2 operates at 1.8 V levels.

3.2.10.4. Coexistence Signals

See section 3.1.12.4, *Coexistence Signals* for a more detailed description of the COEX_TXD, COEX_RXD, and COEX3 signals.

3.2.11. Supplemental Communication-specific Signals

3.2.11.1. FULL_CARD_POWER_OFF#

FULL_CARD_POWER_OFF# is an active low input signal that is used to turn off the entire Adapter ~~module~~. If FULL_CARD_POWER_OFF# is de-asserted (i.e., driven high (≥1.19 V)) the Adapter ~~Module shall~~ must be enabled. If FULL_CARD_POWER_OFF# is asserted (i.e., driven low (≤0.2 V) or Tri-stated), the Adapter ~~module shall~~ must be shut down.

The FULL_CARD_POWER_OFF# pin ~~shall~~ must be pulled low on the Adapter ~~module~~ with a weak pull-down resistor of >20 kΩ. The Adapter ~~module~~ design ~~shall~~ must ensure that the operation of this pin is asynchronous to any other interface operation.

FULL_CARD_POWER_OFF# must be 3.3 V tolerant but ~~may~~ is permitted to be driven by either 1.8 V or 3.3 V GPIO.

3.2.11.2. RESET#

Asynchronous RESET# pin, active low. Whenever this pin is active, the modem will immediately be placed in a Power On reset condition. Care should be taken not to activate this pin unless there is a critical failure and all other methods of regaining control and/or communication with the WWAN sub-system have failed.

! CAUTION: Triggering the RESET# signal will lead to loss of all data in the modem and the removal of system drivers. It will also disconnect the modem from the network.

3.2.11.3. General Purpose Input Output Pins

The GPIO_0 to GPIO_~~–~~11 pins have configurable assignments. There are four possible functional pinouts configurations. These four configurations are called Port Config 0 to Port Config ~~–~~3. In each Port Configuration, each GPIO is defined as a specific functional pin. The GPIO pin assignments are listed in Table 26.

Table 26. GPIO Pin Function Assignment per Port Configuration

	Pin	Port Config_0 (See Note 1)	Port Config_1 (See Note 2)	Port Config_2 (See Note 3)	Port Config_3 (See Note 3)	Note
GPIO_0	40	GNSS_SCL	GNSS_SCL	SIM_DET2	IPC_0	
GPIO_1	42	GNSS_SDA	GNSS_SDA	UIM_DATA2	IPC_1	
GPIO_2	44	GNSS_IRQ	GNSS_IRQ	UIM_CLK2	IPC_2	
GPIO_3	46	SYSCLK	GNSS_0	UIM_RST2	IPC_3	
GPIO_4	48	TX_BLANKING	GNSS_1	UIM_PWR2	IPC_4	
GPIO_5	20	AUDIO_0	AUDIO_0	RFU	AUDIO_0	
GPIO_6	22	AUDIO_1	AUDIO_1	RFU	AUDIO_1	
GPIO_7	24	AUDIO_2	AUDIO_2	RFU	IPC_5/AUDIO_2	
GPIO_8	28	AUDIO_3	AUDIO_3	RFU	IPC_6/AUDIO_3	
GPIO_9	10	LED_1#	LED_1#	LED_1#	DAS/DSS#/IPC_7	5, 6
GPIO_10	26	W_DISABLE2#	W_DISABLE2#	W_DISABLE2#	HSIC_STROBE	
GPIO_11	23	WAKE_ON_WWAN#	WAKE_ON_WWAN#	WAKE_ON_WWAN#	HSIC_DATA	

Notes:

1. GNSS+Audio version 1
2. GNSS+Audio version 2
3. 2nd UIM/SIM Support
4. HSIC Support
5. ~~Platform~~Platform Providers may choose to implement IPC sideband instead of the LED_1# to optimize their design
6. Some host ~~platforms~~ Platforms (eg.,~~x.~~ tablets) may not require support for SSD. In such configurations, Host ~~Platform~~Platform Providers may choose to implement IPC_7 on GPIO_9 instead of DAS/DSS#.

3.2.11.3.1. GNSS Signals

- **GNSS_SCL**
  Input clock for I2C interface for transfer of location data. External device is bus master. For use as a low power interface for location data when host CPU is in low power mode.
- **GNSS_SDA**
  Bi-directional data interface for I2C. For transfer of location data to/from external device (such as a sensor hub).
- **GNSS_IRQ**
  Interrupt signal – bi-~~-~~directional to provide on demand GNSS data to/from external device (such as a sensor hub). Goal ~~i~~is to ~~provide~~provide a low power interface for location data when host CPU is in low power mode.
- **SYSCLK**
  A clock generated by the WWAN Adapter ~~module~~ to provide a means to synchronize the internal WWAN sub system on the WWAN Adapter ~~module~~ to an external GNSS device that ~~may~~ is permitted to reside on the Connectivity Adapter ~~module~~ (e.g., Socket 1) or elsewhere on the ~~platform~~Platform. Used in conjunction with TX_BLANKING signal. Frequency of operation (and clock type) will be dependent on the specific implementation to be used. This is outside the scope of this standard and must be determined as a BTO feature.
- **TX_BLANKING**
  This signal is active high and will be asserted to indicate when the WWAN sub system is engaged in radio transmission activity which would swamp the GNSS signal being received by an off WWAN Adapter ~~module~~ GNSS device. This signal is used in conjunction with SYSCLK signal – specific operation will be dependent on the specific implementation to be used. This is outside the scope of this standard and must be determined as a BTO feature.
- **GNSS_0-1**
  These are pins reserved for proprietary GNSS functions which will be part of BTO on a VENDOR DEFINED basis (see Figure 102).

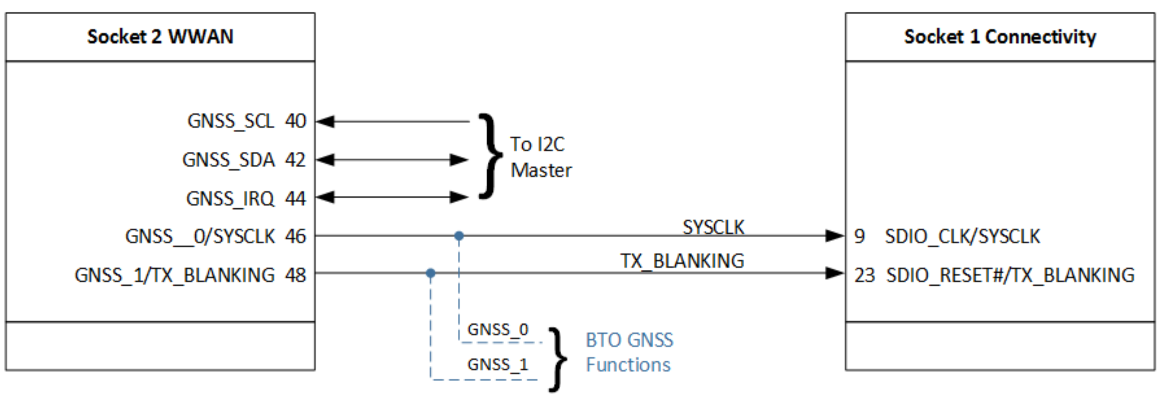


Figure 102. Example of a Connection of the GNSS Signals in a ~~Platform~~Platform Using M.2 Adapter ~~Modules~~

3.2.11.3.2. Audio Signals

AUDIO_0 to AUDIO_~~-~~3 pins are reserved for Audio use. Specific implementations will be part of a BTO option determined specifically by the Adapter ~~module~~ vendor and their customers. Supported options and functions are listed in Table 27.

Table 27. Audio Pin Mode and Function Assignment

M.2 Audio Pins	Pin Mode and Function					
	I2S Mode			SLIMBus Mode		
Pin Name	Function	Direction	Voltage	Function	Direction	Voltage
AUDIO_0	I2S_CLK	I/O	1.8 V	SLIMBus_CLK	O	1.8 V
AUDIO_1	I2S_RX	I	1.8 V	SLIMBus_DAT	I/O	1.8 V
AUDIO_2	I2S_TX	O	1.8 V	Reserved		
AUDIO_3	I2S_WS	I/O	1.8 V	Reserved		

3.2.11.3.3. Second UIM Signals

UIM Interface is used to support Dual SIM operation and consists of the following signals:

- **SIM_DET2, UIM_DATA2, UIM_CLK2, UIM_RST2, UIM_PWR2**
  For specific pin definitions see S~~s~~ection 3.2.9.
- **RFU ~~– Reserved for Future Use~~**
  These pins are not yet assigned as part of this standard but will be allocated as the need arises. These pins cannot be used for any function in this configuration matrix and should be avoided and treated as No Connects at this time.

3.2.11.3.4. IPC[0..7] Signals

These pins ~~may be~~are used for inter-processor communications between the host and the card. The signals assigned to the pins are BTO/CTO.

3.2.11.3.5. WAKE_ON_WWAN# Signal

The WAKE_ON_WWAN# signal is used to wake up the host. It is open drain and needs to be pulled up at the host side. When the WWAN needs to wake up the host, it will output a 1 s~~econd~~ logic low pulse, shown in Figure 103.

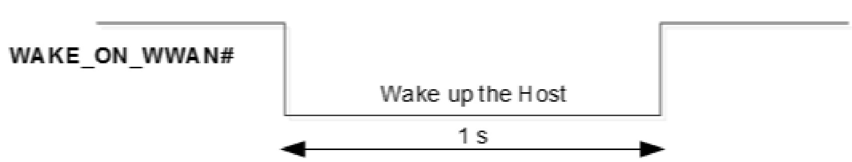


Figure 103. WAKE_ON_WWAN# Signal

3.2.11.4. DPR Signal

The optional Dynamic Power Reduction (DPR)~~ (Dynamic Power Reduction)~~ signal is used by wireless devices to assist in meeting regulatory Specific Absorption Rate (SAR)~~ (Specific Absorption Rate)~~ requirements for RF exposure. The signal is provided by a host system proximity sensor to the wireless device to provide an input trigger causing a reduction in the radio transmit output power.

The required value of the power reduction will vary between different host systems and is left to the host ~~platform~~ Platform OEM and card vendor to determine, along with the specific implementation details. The assertion and de-assertion of DPR is asynchronous to any system clock. All transients resulting from the proximity sensor need to be de-bounced by system circuitry.

3.2.11.5. Antenna Control

ANTCTL~~(~~0 to ANTCTL-3~~)~~ are provided to allow for the implementation of antenna tuning solutions. The number of antenna control lines required will depend on the application and antenna/band requirements.

The functional definition of the antenna control pins ~~are~~ is OEM-specific and should be coordinated between the host ~~platform~~ Platform OEM and card vendors. The ordered labeling of these signals in this specification is intended to help establish consistent implementations—where practical—across multiple instances of cards in the host ~~platform~~Platform. Supported options are listed in Table 28.

Table 28. Antenna Control Pin Mode and Function Assignment

M.2 Antenna Control	Pin Mode and Function							
	GPIO Mode			RFFE Mode			
Pin Name	Function	Direction	Voltage	Function	Direction	Voltage	Note
ANTCTL0	GPIO_0 (LSB)	O	1.8 V	Reserved			1
ANTCTL1	GPIO_1	O	1.8 V	RFFE_SDATA	I/O	1.8 V	1
ANTCTL2	GPIO_2	O	1.8 V	RFFE_SCLK	O	1.8 V	1
ANTCTL3	GPIO_3 (MSB)	O	1.8 V	RFFE_VIO	O	1.8 V	1

Note 1: In GPIO Mode operating voltage for pins is 1.8 V Nominal, BUT is permitted to be up to 2.8 V to allow direct operation of antenna controllers using multiple silicon technologies.

3.2.12. SSD Specific Signals

3.2.12.1. Reserved for MFG CLOCK and DATA

There are two Adapter ~~module~~ pins that are dedicated as SSD Manufacturing pins. Their purpose is dependent on implementation of the vendor. These pins must be ~~no-connect~~NC on the ~~motherboard~~Motherboard.

3.2.12.2. SMBus Interface

The SMBus interface supported in SSD Socket 2 is intended as optional side band management interface for SSD applications. SMBus is a three-wire interface (ALERT# signal is optional) through which various system component chips communicate with each other and with rest of the system. It is based on the principles of operation of I2C. Refer to the *SMBus Specification* for details of the operation.

3.2.12.2.1. ALERT# Signal

The ALERT# signal is intended to indicate to the ~~platform~~Platform~~/system~~ that the SMBus device requires attention. This GPIO ~~can be~~ is used to establish specific communication/signaling to the host from the device. This signal is Active Low.

3.2.12.2.2. SMB_DATA Signal

The SMB_DATA signal is used to transfer the data packets between the host and the device per the SMBus protocol. The speed supported on this line depends on the host SMB_CLK signal speeds and the device processing capability.

3.2.12.2.3. SMB_CLK Signal

The SMB_CLK signal provides the clock signaling from the SMBus master to the SMBus slave device to be able to decode the data on the SMB_DATA line.

3.2.13. Configuration Pins

Socket 2 Key B pinout incorporates four configuration pins which ~~can~~ assist the ~~platform~~ Platform to identify the presence of an Add-~~i~~In Card in the socket and identify card Type, ~~Host I/F~~host interface it utilizes, and, in the case of WWAN, Port Configuration for the GPIO_0 to GPIO~~–~~_11 interface pins.

The operation of this configuration interface is as follows:

- Pins CONFIG_0..3
  These pins are grounded or left NC on the ~~Module~~ Add-in Card per the desired configuration attached to the Host device when plugged into the Socket 2. All configuration pins should be read and decoded by the host ~~platform~~ Platform to recognize the indicated Add-in Card ~~module~~ configuration and host interface supported as listed in Table 29.
- On the ~~platform~~Platform side, each of the CONFIG_0..3 signals needs to be fitted with a pull-up resistor. Based on the state of the configuration pins on the Add-in Card ~~module~~, being tied to

GND or left No Connect (NC), the sensed pins will create a 4-bit logic state that require decoding.

- This configuration scheme will ensure that an Add-in Card ~~module~~ and its configuration ~~can~~ is always ~~be~~ detected.

Table 29. Socket 2 Add-in Card ~~Module~~ Configuration

State #	Add-in Card ~~Module~~ Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Add-in Card ~~Module~~ Type and Main Host Interface~~1~~ (see Note 1)	Port Configuration ~~2~~ (see Note 2)
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	NC	GND	GND	SSD – PCIe	N/A
2	GND	GND	NC	GND	WWAN – PCIe	0
3	GND	NC	NC	GND	WWAN – PCIe	1
4	GND	GND	GND	NC	WWAN – USB3.1 Gen1	0
5	GND	NC	GND	NC	WWAN – USB3.1 Gen1	1
6	GND	GND	NC	NC	WWAN – USB3.1 Gen1	2
7	GND	NC	NC	NC	WWAN – USB3.1 Gen1	3
8	NC	GND	GND	GND	WWAN – SSIC	0
9	NC	NC	GND	GND	WWAN – SSIC	1
10	NC	GND	NC	GND	WWAN – SSIC	2
11	NC	NC	NC	GND	WWAN – SSIC	3
12	NC	GND	GND	NC	WWAN – PCIe	2
13	NC	NC	GND	NC	WWAN – PCIe	3
14	NC	GND	NC	NC	RFU	N/A
15	NC	NC	NC	NC	No Add-in Card ~~Module~~ Present	N/A

Notes:

1 USB 2.0 supported on all WWAN configurations (HSIC supported on WWAN configuration 3)

2 Applicable to WWAN only

3.2.14. Vendor Defined Pins

Socket 2 incorporates 14 Vendor defined pins arranged in the following three pin location groupings in the pinout:

- VENDOR_PORT_A (four pins)
- VENDOR_PORT_B (six pins)
- VENDOR_PORT_C (four pins)

While these ports have been grouped in the pinout to enable potential functional groupings, it should be noted that all these pins are fully vendor defined in a BTO agreement between the customer and vendor. Alternate arrangements with or without groupings are possible to enable any desired functionality using 14 vendor-defined signals.

Typically, these pins are assumed to be GPIO that are at 1.8 V I/O level. However, it is possible to define vendor defined pins as host interface signals that ~~may~~ have other associated voltage levels with the desired signals.

Some of the vendor defined pins (specifically the VENDOR_PORT_C pins) have been placed strategically between GND pins to enable optimized differential signal operation with improved isolation from adjacent signals.

The 14 allocated vendor-defined pins provide many potential combinations of features and functions that ~~can be~~are implemented using these signals in a BTO mode of operation and agreement between customer and vendor. Some examples are given in the Annex.

3.2.15. Socket 2 Connector Pinout Definitions

> All pinouts tables in this section are written from the ~~module~~ Adapter point of view when referencing signal directions.

3.2.15.1. Socket 2 Key B Pinout Definitions

The following tables list the signal pinouts for the Adapter ~~module~~ edge card connector:

- Table 30. Socket 2 Key B SSIC-based WWAN Adapter Pinouts
- Table 31. Socket 2 Key B USB3.1 Gen1-based WWAN Adapter Pinout
- Table 32. Socket 2 Key B PCIe-based WWAN Adapter Pinout

All three of these WWAN pinouts also support legacy USB2.0-based WWAN solutions or optionally HSIC.

See Table 29 for a list of Socket 2 configuration bits on the Add-in Card ~~Module~~ used to identify the desired pinouts and Port Configuration.

Table 33 lists the SATA-based SSD solution and Table 34 lists the PCIe Multi-lane based SSD solution.

The pinouts in Table 33 and Table 34 utilize a dual Add-in Card ~~module~~ key scheme to enable these solutions to also plug into a Socket 3 connector if available in the ~~platform~~Platform. The CONFIG_1 pin in these pinouts is equivalent to the PEDET signal used in Socket 3.

Table 30. Socket 2 Key B SSIC-based WWAN Adapter ~~Module~~ Pinouts

Pin	Signal	Signal	Pin
74	3.3 V	CONFIG_2 (States 8, 9, 10, 11)	75
72	3.3 V	GND	73
70	3.3 V	GND	71
68	SUSCLK(32kHz) (I)(0/3.3V)	CONFIG_1 (States 8, 9, 10, 11)	69
66	SIM_DETECT (I)	RESET# (I)(0/1.8V)	67
64	COEX_TXD (O)(0/1.8V)	ANTCTL3 (O)(0/1.8V)	65
62	COEX_RXD (I)(0/1.8V)	ANTCTL2 (O)(0/1.8V)	63
60	COEX3 (I/O)(0/1.8V)	ANTCTL1 (O)(0/1.8V)	61
58	NC	ANTCTL0 (O)(0/1.8V)	59
56	NC	GND	57
54	NC	NC	55
52	NC	NC	53
50	NC	GND	51
48	GPIO_4 - TX_BLANKING/GNSS_1/UIM_ PWR2/IPC_4 (I/O)(0/1.8V)	NC	49
46	GPIO_3 - SYSCLK/GNSS_0/UIM_RST2/IPC_3 (I/O)(0/1.8V)	NC	47
44	GPIO_2 - GNSS_IRQ/GNSS_IRQ/UIM_CLK2/IPC_2 (I/O)(0/1.8V)	GND	45
42	GPIO_1 - GNSS_SDA/GNSS_SDA/UIM_ DATA2/IPC_1 (I/O)(0/1.8V)	NC	43
40	GPIO_0 - GNSS_SCL/GNSS_SCL/SIM_ DET2/IPC_0 (I/O)(0/1.8V)	NC	41
38	NC	GND	39
36	UIM_PWR (O)	SSIC-RxP	37
34	UIM_DATA (I/O)	SSIC-RxN	35
32	UIM_CLK (O)	GND	33
30	UIM_RESET (O)	SSIC-TxP	31
28	GPIO_8 - AUDIO_3/AUDIO_3/RFU/IPC_6-AUDIO_3 (I/O) (0/1.8V)	SSIC-TxN	29
26	GPIO_10 - W_DISABLE2#/W_DISABLE2#/W_DISABLE2# (I/O) (0/1.8V) /HSIC_STROBE (I/O) (0/1.2V)	GND	27
24	GPIO_7 - AUDIO_2/AUDIO_2/RFU/IPC_5-AUDIO_2 (I/O) (0/1.8V)	DPR (I)(0/1.8V)	25
22	GPIO_6 - AUDIO_1/AUDIO_1/RFU/AUDIO_1 (I/O)(0/1.8V)	GPIO_11 - WoWWAN#/WoWWAN#/WoWWAN# (O)(0/1.8V)/HSIC_DATA (I/O)(0/1.2V)	23
20	GPIO_5 - AUDIO_0/AUDIO_0/RFU/AUDIO_0 (I/O)(0/1.8V)	CONFIG_0 = NC	21
	~~MODULE~~ ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
10	GPIO_9 - LED_1#/LED_1#/LED_1# (O)(OD)(0/3.3V) /IPC_7 (I/O)(0/1.8V)	GND	11
8	W_DISABLE1# (I)(0/3.3V)	USB_D-	9
6	FULL_CARD_POWER_OFF# (I)(0/1.8V or 3.3V)	USB_D+	7
4	3.3 V	GND	5
2	3.3 V	GND	3
		CONFIG_3 = GND	1

Table 31. Socket 2 Key B USB3.1 Gen1-based WWAN ~~Module~~ Adapter Pinout

Pin	Signal	Signal	Pin
		CONFIG_2 (States 4, 5, 6, 7)	75
74	3.3 V	GND	73
72	3.3 V	GND	71
70	3.3 V	CONFIG_1 (States 4, 5, 6, 7)	69
68	SUSCLK(32kHz) (I)(0/3.3V)	RESET# (I)(0/1.8V)	67
66	SIM_DETECT (I)	ANTCTL3 (O)(0/1.8V)	65
64	COEX_TXD (O)(0/1.8V)	ANTCTL2 (O)(0/1.8V)	63
62	COEX_RXD (I)(0/1.8V)	ANTCTL1 (O)(0/1.8V)	61
60	COEX3 (I/O)(0/1.8V)	ANTCTL0 (O)(0/1.8V)	59
58	NC	GND	57
56	NC	NC	55
54	NC	NC	53
52	NC	GND	51
50	NC	NC	49
48	GPIO_4 - TX_BLANKING/GNSS_1/UIM_ PWR2/IPC_4 (I/O)(0/1.8V)	NC	47
46	GPIO_3 - SYSCLK/GNSS_0/UIM_RST2/IPC_3 (I/O)(0/1.8V)	GND	45
44	GPIO_2 - GNSS_IRQ/GNSS_IRQ/UIM_ CLK2/IPC_2 (I/O)(0/1.8V)	NC	43
42	GPIO_1 - GNSS_SDA/GNSS_SDA/UIM_ DATA2/IPC_1 (I/O)(0/1.8V)	NC	41
40	GPIO_0 - GNSS_SCL/GNSS_SCL/SIM_ DET2/IPC_0 (I/O)(0/1.8V)	GND	39
38	NC	USB3.1-Rx+	37
36	UIM-PWR (O)	USB3.1-Rx-	35
34	UIM-DATA (IO)	GND	33
32	UIM-CLK (O)	USB3.1-Tx+	31
30	UIM-RESET (O)	USB3.1-Tx-	29
28	GPIO_8 - AUDIO_3/AUDIO_3/RFU/IPC_6-AUDIO_3 (I/O) (0/1.8V)	GND	27
26	GPIO_10 - W_DISABLE2#/W_DISABLE2#/W_ DISABLE2# (I/O) (0/1.8V)/HSIC_STROBE (I/O) (0/1.2V)	DPR (I)(0/1.8V)	25
24	GPIO_7 - AUDIO_2/AUDIO_2/RFU/IPC_5-AUDIO_2 (I/O) (0/1.8V)	GPIO_11-WoWWAN#/WoWWAN#/WoWWAN# (O)(0/1.8V)/HSIC_DATA (I/O)(0/1.2V)	23
22	GPIO_6 - AUDIO_1/AUDIO_1/RFU/AUDIO_1 (I/O)(0/1.8V)	CONFIG_0 = GND	21
20	GPIO_5 - AUDIO_0/AUDIO_0/RFU/AUDIO_0 (I/O)(0/1.8V)	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	GND	11
10	GPIO_9 - LED_1#/LED_1#/LED_1# (O)(OD)(0/3.3V) /IPC_7 (I/O)(0/1.8V)	USB_D-	9
8	W_DISABLE1# (I)(0/3.3V)	USB_D+	7
6	FULL_CARD_POWER_OFF# (I)(0/1.8V)	GND	5
4	3.3 V	GND	3
2	3.3 V	CONFIG_3 = NC	

Pin	Signal	Signal	Pin

Table 32. Socket 2 Key B PCIe-based WWAN ~~Module~~ Adapter Pinout

Pin	Signal	Signal	Pin
		CONFIG_2 (States 2, 3, 12, 13)	75
74	3.3 V	GND	73
72	3.3 V	GND	71
70	3.3 V	CONFIG_1 (States 2, 3, 12, 13)	69
68	SUSCLK(32kHz) (I)(0/3.3V)	RESET# (I)(0/1.8V)	67
66	SIM_DETECT (I)	ANTCTL3 (O)(0/1.8V)	65
64	COEX_TXD (O)(0/1.8V)	ANTCTL2 (O)(0/1.8V)	63
62	COEX_RXD (I)(0/1.8V)	ANTCTL1 (O)(0/1.8V)	61
60	COEX3 (I/O)(0/1.8V)	ANTCTL0 (O)(0/1.8V)	59
58	NC	GND	57
56	NC	REFCLKp	55
54	PEWAKE# (I/O)(0/3.3V)	REFCLKn	53
52	CLKREQ# (I/O)(0/3.3V)	GND	51
50	PERST# (I)(0/3.3V)	PERp0	49
48	GPIO_4 - TX_BLANKING/GNSS_1/UIM_PWR2/IPC_4 (I/O)(0/1.8V*)	PERn0	47
46	GPIO_3 - SYSCLK/GNSS_0/UIM_RST2/IPC_3 (I/O)(0/1.8V*)	GND	45
44	GPIO_2 - GNSS_IRQ/GNSS_IRQ/UIM_CLK2/IPC_2 (I/O)(0/1.8V*)	PETp0	43
42	GPIO_1 - GNSS_SDA/GNSS_SDA/UIM_DATA2/IPC_1 (I/O)(0/1.8V*)	PETn0	41
40	GPIO_0 - GNSS_SCL/GNSS_SCL/SIM_DET2/IPC_0 (I/O)(0/1.8V*)	GND	39
38	NC	PERp1	37
36	UIM-PWR (O)	PERn1	35
34	UIM-DATA (I/O)	GND	33
32	UIM-CLK (O)	PETp1	31
30	UIM-RESET (O)	PETn1	29
28	GPIO_8 - AUDIO_3/AUDIO_3/RFU/IPC_6-AUDIO_3 (I/O) (0/1.8V)	GND	27
26	GPIO_10 - W_DISABLE2#/W_DISABLE2#/W_DISABLE2# (I/O)(0/1.8V)/HSIC_STROBE (I/O) (0/1.2V)	DPR (I)(0/1.8V)	25
24	GPIO_7 - AUDIO_2/AUDIO_2/RFU/IPC_5-AUDIO_2 (I/O) (0/1.8V)	GPIO_11 - WoWWAN#/WoWWAN#/WoWWAN# (O)(0/1.8V)/HSIC_DATA (I/O)(0/1.2V)	23
22	GPIO_6 - AUDIO_1/AUDIO_1/RFU/AUDIO_1 (I/O)(0/1.8V)	CONFIG_0 (States 2, 3, 12, 13)	21
20	GPIO_5 - AUDIO_0/AUDIO_0/RFU/AUDIO_0 (I/O)(0/1.8V)	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	GND	11
10	GPIO_9 - LED_1#/LED_1#/LED_1# (O)(OD)(0/3.3V) /IPC_7 (I/O)(0/1.8V)	USB_D-	9
8	W_DISABLE1# (I)(0/3.3V)	USB_D+	7
6	FULL_CARD_POWER_OFF# (I)(0/1.8V)	GND	5
4	3.3 V	GND	3
2	3.3 V	CONFIG_3 (States 2, 3, 12, 13)	1

Table 33. Socket 2 Key B-M SATA-based SSD ~~Module~~ Adapter Pinout

Pin	Signal	Signal	Pin
74	3.3V	CONFIG_2 = GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (I)(0/3.3V)	CONFIG_1 = GND	69
	ADD-IN CARD KEY M	NC	67
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
58	Reserved for MFG_CLOCK	ADD-IN CARD KEY M	
56	Reserved for MFG_DATA	GND	57
54	NC	NC	55
52	NC	NC	53
50	NC	GND	51
48	NC	SATA-A+	49
46	NC	SATA-A-	47
44	ALERT# (O)(0/1.8V)	GND	45
42	SMB_DATA (I/O)(0/1.8V)	SATA-B-	43
40	SMB_CLK (I/O)(0/1.8V)	SATA-B+	41
38	DEVSLP (I)	GND	39
36	NC	NC	37
34	NC	NC	35
32	NC	GND	33
30	NC	NC	31
28	NC	NC	29
26	NC	GND	27
24	NC	NC	25
22	NC	NC	23
20	NC	CONFIG_0 = GND	21
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
10	DAS/DSS# (I/O)	NC	11
8	NC	NC	9
6	NC	NC	7
4	3.3V	NC	5
2	3.3V	GND	3

Pin	Signal	Signal	Pin
		CONFIG_3 = GND	1

Table 34. Socket 2 Key B-M PCIe-based SSD ~~Module~~ Adapter Pinout

Pin	Signal	Signal	Pin
		CONFIG_2 = GND	75
74	3.3 V	GND	73
72	3.3 V	GND	71
70	3.3 V	CONFIG_1 = NC	69
68	SUSCLK(32kHz) (I)(0/3.3V)	NC	67
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
	ADD-IN CARD KEY M	ADD-IN CARD KEY M	
58	Reserved for MFG_CLOCK	GND	57
56	Reserved for MFG_DATA	REFCLKp	55
54	PEWAKE# (I/O)(0/3.3V)	REFCLKn	53
52	CLKREQ# (I/O)(0/3.3V)	GND	51
50	PERST# (I)(0/3.3V)	PERp0	49
48	NC	PERn0	47
46	NC	GND	45
44	ALERT# (O)(0/1.8V)	PETp0	43
42	SMB_DATA (I/O)(0/1.8V)	PETn0	41
40	SMB_CLK (I/O)(0/1.8V)	GND	39
38	NC	PERp1	37
36	NC	PERn1	35
34	NC	GND	33
32	NC	PETp1	31
30	NC	PETn1	29
28	NC	GND	27
26	NC	NC	25
24	NC	NC	23
22	NC	CONFIG_0 = GND	21
20	NC	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	ADD-IN CARD KEY B	
	ADD-IN CARD KEY B	NC	11
10	LED_1#	NC	9
8	NC	NC	7
6	NC	NC	5
4	3.3 V	GND	3

Pin	Signal	Signal	Pin
2	3.3 V	CONFIG_3 = GND	1

3.2.15.2. Socket 2 Key C Pinout Definitions

Table 35. Socket 2 Key C WWAN ~~Module~~ Adapter Pinout

Pin	Signal	Signal	Pin
		GND	75
74	3.3 V	GND	73
72	3.3 V	RESET# (I) (0/1.8V)	71
70	ANTCTL3 GPIO_3 (MSB) (O)/RFFE_VIO (O) (0/1.8V)	COEX_TXD (O) (0/1.8V)	69
68	ANTCTL2 GPIO_2 (O)/REF_SCLK (O) (0/1.8V)	COEX_RXD (I) (0/1.8V)	67
66	ANTCTL1 GPIO_1 (O)/REF_SDATA (I/O) (0/1.8V)	GND	65
64	ANTCTL0 GPIO_0 (O) (0/1.8V)	VENDOR_PORT_C_3	63
62	RESERVED	VENDOR_PORT_C_2	61
60	VENDOR_PORT_B_5	GND	59
58	VENDOR_PORT_B_4	VENDOR_PORT_C_1	57
56	RESERVED	VENDOR_PORT_C_0	55
54	VENDOR_PORT_B_3	GND	53
52	VENDOR_PORT_B_2	M/REFCKLP	51
50	VENDOR_PORT_B_1	MREFCLKN	49
48	VENDOR_PORT_B_0	GND	47
46	PEWAKE# (I/O) (0/1.8V)	M/PERp0; SSIC-RxP; USB3.1-Rx+	45
44	CLKREQ# (I/O) (0/1.8V)	M/PERn0; SSIC-RxN; USB3.1-Rx-	43
42	PERST# (I) (0/1.8V)	GND	41
40	SIM DETECT2 (I) (0/1.8V)	M/PETp0; SSIC-TxP; USB3.1-Tx+	39
38	UIM2-PWR (O)	M/PERn0; SSIC-TxN; USB3.1-Tx-	37
36	UIM2-DATA (I/O)	GND	35
34	UIM2-CLK (O)	SIM DETECT1 (I) (0/1.8V)	33
32	UIM2-RESET (O)	UIM1_PWR (O)	31
30	AUDIO1 I2S_WS (I/O) (0/1.8V)	UIM1_DATA (I/O)	29
28	AUDIO1 I2S_TX (O) (0/1.8V)	UIM1_CLK (O)	27
26	AUDIO1 I2S_RX (I) SLIMUS_DAT (I/O) (0/1.8V)	UIM1_RESET (O)	25
24	AUDIO1 I2S_CLK (I/O) SLIMUS_CLK (I/O) (0/1.8V)	ADD-IN CARD KEY C	
	ADD-IN CARD KEY C	ADD-IN CARD KEY C	
	ADD-IN CARD KEY C	ADD-IN CARD KEY C	
	ADD-IN CARD KEY C	ADD-IN CARD KEY C	
	ADD-IN CARD KEY C	VIO1.8V	15
20	VENDOR_PORT_A_3	FULL_CARD_POWER_OFF# (I) (0/1.8V)	13
12	VENDOR_PORT_A_2	DPR (I) (0/1.8V)	11
10	VENDOR_PORT_A_1		

Pin	Signal	Signal	Pin
8	VENDOR_PORT_A_0	GND	9
6	3.3 V	USB_D-	7
4	3.3 V	USB_D+	5
2	3.3 V	GND	3
		GND	1

3.3. SSD Socket 3 ~~Module~~ Adapter Interface Signals

Table 36 ~~Table 36~~ contains a list of the Socket 3 ~~module~~ Adapter interface signals.

Table 36. Socket 3 System Interface Signal Table

Interface	Signal Name	I/O	Function	Voltage
Power and Grounds	~~+~~3.3 V (9 pins)	I	3.3 V source.	3.3 V
	GND (14 pins)		Return current path.	0 V
PCIe	PERp0, PERn0/ PETp0, PETn0 PERp1, PERn1/ PETp1, PETn1 PERp2, PERn2/ PETp2, PETn2 PERp3, PERn3/ PETp3, PETn3	I/O	PCIe TX/RX Differential signals defined by the *PCI Express CEM Specification*.	
	REFCLKp/ REFCLKn	I	PCIe Reference Clock signals (100 MHz) defined by the *PCI Express CEM Specification*.	
	PERST#	I	PCIe Reset is a functional reset to the card as defined by the *PCIe Mini CEM Specification*.	3.3 V
	CLKREQ#	I/O	Clock Request is a reference clock request signal as defined by the *PCI Express ~~PCIe~~ Mini CEM S~~s~~pecification*; Open Drain with pull up on ~~platform~~Platform; Active Low; ~~Also~~ also used by L1 PM Substates.	3.3 V
	PEWAKE#/OBFF	I/O	PCIe WAKE#. Open Drain with pull up on ~~platform~~Platform. Active Low when used as PEWAKE#. When the ~~add-in module~~Adapter supports wakeup, this signal is used to request that the system return from a sleep/suspend state to service a function initiated wake event. When the ~~add-in module~~Adapter supports OBFF mechanism, the signal is used by the system to indicate OBFF or CPU Active State transitions.	3.3 V
SATA	SATA-A+, SATA-A-/SATA-B+, SATA-B-	I/O	Refer to the *Serial ATA Specification.*	
	DEVSLP	I		
	DAS/DSS#	I/O		
SSD Specific Signals	SUSCLK	I	32.768 kHz clock supply input that is provided by the ~~platform~~ Platform chipset to reduce power and cost for the ~~module~~Adapter. SUSCLK duty cycle is permitted to be as low as 30% or as high as 70%. The tolerance for this clock is ±100 ppm~~SUSCLK will have a duty cycle that can be as low as 30% or as high as 70%. 200 ppm~~.	3.3 V
	PEDET	O	Host interface~~I/F~~ Indication; To be grounded for SATA, No Connect for PCIe.	0 V or ~~/~~NC

Interface	Signal Name	I/O	Function	Voltage
	Reserved for MFG_DATA		Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left NC in ~~platform~~ Platform Socket.	
	Reserved for MFG_CLOCK		Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left NC in ~~platform~~ Platform Socket.	
	LED_1#	O	Open drain, active low signal. This signal is used to allow the Adapter ~~add-in card~~ to provide status indication via LED device that will be provided by the system.	3.3 V
	ALERT#	O	Alert notification to master; Open Drain with pull up on ~~platform~~Platform; Active Low	1.8 V
	SMB_CLK	I/O	SMBus clock; Open Drain with pull up on ~~platform~~Platform	1.8 V
	SMB_DATA	I/O	SMBus clock; Open Drain with pull up on P~~p~~latform	1.8 V

3.3.1. Power and Grounds

PCI Express M.2 Socket 3 utilizes a single 3.3 V power source similar to that of Socket 1 and 2. The voltage source, ~~+~~3.3 V, is expected to be available during the system's stand-by/suspend state to support wake event processing on the communications card. In socket 3, there is provision for nine 3.3 V pins to enable high continuous current, the same as in Socket 2 if required. The higher number of pins will help to reduce further the current resistance (IR) drop on the connector.

Some of the higher frequency signals require additional isolation from surrounding signals using the concept of interleaving ~~ground (~~GND~~)~~ pins separating signals within the connector. These pins should be treated as a normal ground pin with connections immediately made to the ground planes within a card design.

3.3.2. PCI Express Interface

The PCI Express interface supported in Socket 3 is a four lane PCI Express interface intended for premium SSD devices that need this sort of host interface. Socket 3 ~~can~~ also supports SSD devices that make use of only two lanes PCI Express and are plugged in to Socket 2 with the aid of a Dual ~~Module~~ Add-in Card key. See S~~s~~ection 3.1.2 ~~in this specification~~ for a detailed description of the PCIe signals.

3.3.3. SATA Interface (Informative)

SATA is a high-speed serialized ATA data link interface (specifying Phy, Link, Transport, and Application layers) for hard and solid state drives as defined by the Serial ATA International Organization (refer to the *Serial ATA Specification*).

3.3.3.1. DEVSLP

The DEVSLP ~~(Device Sleep)~~ pin is used to inform a SATA Device that it should enter a DEVSLP ~~DevSleep~~ Interface Power state (refer to the *Serial ATA Specification*).

3.3.3.2. DAS/DSS#

The DAS ~~(Drive Activity Signal)~~ is driven by the SATA device to indicate that an access is occurring. Hosts ~~may~~ are also permitted to use the same signal for DSS# ~~(Disable Staggered Spin-up)~~ and other functions (refer to the *Serial ATA Specification*).

3.3.4. SSD Specific Signals

3.3.4.1. SUSCLK

See ~~S~~section 3.1.12.1 ~~in this specification~~ for a detailed description of the SUSCLK ~~(Suspend Clock)~~ signal.

3.3.4.2. PEDET

The interface detect ~~can be~~is used by the host computer to determine the communication protocol that the M.2 Adapter ~~card~~ uses; SATA signaling (low) or PCIe signaling (high) in conjunction with a ~~platform~~ Platform located pull-up resistor.

3.3.4.3. Reserved for MFG Clock ~~&~~and Data

There are two Adapter ~~module~~ pins that are dedicated as SSD Manufacturing pins. Their purpose is dependent on implementation of the vendor. These pins must be no-connect on the ~~motherboard~~motherboard.

3.3.4.4. Status Indicators (LED_1#)

See section 3.1.12.2, Status Indicators, for a more detailed description of the LED_1# signal.

3.3.4.5. SMBus Interface

The SMBus interface supported in SSD Socket 3 is intended as optional side band management interface for SSD applications. See section 3.2.12.2, SMBus Interface, in this specification for more information.

3.3.5. Socket 3 Connector Pinout Definitions

> All pinouts tables in this section are written from the Adapter ~~module~~ point of view when referencing signal directions.

Table 37 and Table 38 list the signal pinouts for the Add-in Card ~~module~~ edge card connector. Table 37 lists the SATA based solution pinouts. Table 38 lists the PCIe Multi-lane based solution pinouts.

Table 37. Socket 3 SATA-based Adapter ~~Module~~ Pinouts (~~Module~~ Key M)

Pin	Signal	Signal	Pin
		GND	75
74	3.3V	GND	73
72	3.3V	GND	71
70	3.3V	PEDET (GND-SATA)	69
68	SUSCLK(32kHz) (I)(0/3.3V)	NC	67
	~~CONNECTOR~~ ADD_IN CARD KEY M	ADD_IN CARD KEY M~~CONNECTOR KEY M~~	
	ADD_IN CARD KEY M~~CONNECTOR KEY M~~	ADD_IN CARD KEY M~~CONNECTOR KEY M~~	
	ADD_IN CARD KEY M~~CONNECTOR KEY M~~	ADD_IN CARD KEY M~~CONNECTOR KEY M~~	
	ADD_IN CARD KEY M~~CONNECTOR KEY M~~	ADD_IN CARD KEY M~~CONNECTOR KEY M~~	
58	Reserved for MFG_CLOCK	GND	57
56	Reserved for MFG_DATA	NC	55
54	NC	NC	53
52	NC	GND	51
50	NC	SATA-A+	49
48	NC	SATA-A-	47
46	NC	GND	45
44	ALERT# (O) (0/1.8V)	SATA-B-	43
42	SMB_DATA (I/O) (0/1.8V)	SATA-B+	41
40	SMB_CLK (I/O) (0/1.8V)	GND	39
38	DEVSLP (I)	NC	37
36	NC	NC	35
34	NC	GND	33
32	NC	NC	31
30	NC	NC	29
28	NC	GND	27
26	NC	NC	25
24	NC	NC	23
22	NC	GND	21
20	NC	NC	19
18	3.3V	NC	17
16	3.3V	GND	15
14	3.3V	NC	13
12	3.3V	NC	11
10	DAS/DSS# (I/O)	GND	9
8	NC	NC	7
6	NC	NC	5
4	3.3V	GND	3
2	3.3V	GND	1

Table 38. Socket 3 PCIe-based ~~Module~~ Adapter Pinouts (~~Module~~ Key M)

Pin	Signal	Signal	Pin
		GND	75
74	3.3V	GND	73
72	3.3V	GND	71
70	3.3V	PEDET (NC-PCIe)	69
68	SUSCLK(32kHz) (I)(0/3.3V)	NC	67
	ADD_IN CARD KEY M~~CONNECTOR KEY M~~	ADD_IN CARD KEY M~~CONNECTOR KEY M~~	
	ADD_IN CARD KEY M~~CONNECTOR KEY M~~	ADD_IN CARD KEY M~~CONNECTOR KEY M~~	
	ADD_IN CARD KEY M~~CONNECTOR KEY M~~	ADD_IN CARD KEY M~~CONNECTOR KEY M~~	
	ADD_IN CARD KEY M~~CONNECTOR KEY M~~	ADD_IN CARD KEY M~~CONNECTOR KEY M~~	
58	Reserved for MFG_CLOCK	GND	57
56	Reserved for MFG_DATA	REFCLKp	55
54	PEWAKE# (I/O)(0/3.3V)	REFCLKn	53
52	CLKREQ# (I/O)(0/3.3V)	GND	51
50	PERST# (I)(0/3.3V)	PERp0	49
48	NC	PERn0	47
46	NC	GND	45
44	ALERT# (O)(0/1.8V)	PETp0	43
42	SMB_DATA (I/O)(0/1.8V)	PETn0	41
40	SMB_CLK (I/O)(0/1.8V)	GND	39
38	NC	PERp1	37
36	NC	PERn1	35
34	NC	GND	33
32	NC	PETp1	31
30	NC	PETn1	29
28	NC	GND	27
26	NC	PERp2	25
24	NC	PERn2	23
22	NC	GND	21
20	NC	PETp2	19
18	3.3V	PETn2	17
16	3.3V	GND	15
14	3.3V	PERp3	13
12	3.3V	PERn3	11
10	LED_1# (O)	GND	9
8	NC	PETp3	7
6	NC	PETn3	5
4	3.3V	GND	3

Pin	Signal	Signal	Pin
2	3.3V	GND	1

3.4. BGA SSD Interface Signals

Table 39 contains a list of the signals defined for BGA SSDs. The I/O direction indicated is from BGA ~~module's~~ Adapter's perspective.

Table 39. BGA SSD System Interface Signal Table

Interface	Signal Name	I/O	Function	Voltage
Power and Grounds	~~+3~~3.3 V (8 pins)	I	3.3 V source	3.3 V
	~~+~~1.8 V (12 pins)	I	1.8 V source	1.8 V
	~~+~~1.2 V (12 pins)	I	1.2 V source	1.2 V
	GND (104 pins)		Return current path	0 V
PCIe	PERp0, PERn0/ PETp0, PETn0 PERp1, PERn1/ PETp1, PETn1 PERp2, PERn2/ PETp2, PETn2 PERp3, PERn3/ PETp3, PETn3	I/O	PCIe TX/RX Differential signals defined by the *PCI Express Card Electromechanical Specification*.	
	REFCLKp/ REFCLKn	I	PCIe Reference Clock signals (100 MHz) defined by the *PCI Express Card Electromechanical Specification*. ~~Note:~~ This reference clock is the common ref clock that ~~shall~~ must be used with PCIe.	
	PERST#	I	PE-Reset is a functional reset to the card as defined by the *PCI Express Mini Card Electromechanical Specification*.	1.8 V
	CLKREQ#	I/O	Clock Request is a reference clock request signal as defined by the *PCI Express Mini Card Electromechanical Specification*; Also used by L1 PM Substates.	1.8 V
	PEWAKE#/OBFF	I/O	PCIe WAKE#. Open Drain with pull up on ~~platform~~Platform. Active Low when used as PEWAKE#. When the Adapter ~~add-in module~~ supports wakeup, this signal is used to request that the system return from a sleep/suspend state to service a function initiated wake event. When the Adapter ~~add-in module~~ supports OBFF mechanism, the signal is used by the system to indicate OBFF or CPU Active State transitions.	1.8 V

Interface	Signal Name	I/O	Function	Voltage
SATA	SATA-A+, SATA-A-/ SATA-B+, SATA-B-	I/O	Refer to *Serial ATA Specification*.	
	DEVSLP	I		
	DAS/DSS#	I/O		
SSD Specific Signals	SUSCLK	I	32.768 kHz clock supply input provided by the ~~platform~~ Platform chipset to reduce power and cost for the Adapter~~module~~. SUSCLK duty cycle is permitted to be as low as 30% or as high as 70%. ~~SUSCLK will have a duty cycle that can be as low as 30% or as high as 70%.~~ The tolerance for this clock is ±100 ppm.	1.8 V
	PEDET	O	Host ~~I/F~~interface Indication; To be grounded for SATA, No Connect for PCIe.	0 V or ~~/~~NC
	RFU		Reserved for future use.	
	DNU		Do not use. Manufacturing purpose only.	
SSD Specific Optional Signals	XTAL_IN	I	Connection to crystal unit.	
	XTAL_OUT	O	Connection to crystal unit.	
	CAL_P	N/A	PHY calibration resistor.	
	RZQ_1, RZQ_2	N/A	Memory or NAND calibration resistor.	
	JTAG_TRST#	I	Refer to *JTAG Specification (IEEE 1149.1), Test Access Port and Boundary Scan Architecture* for definition of these balls.	3.3 V
	JTAG_TCK	I		
	JTAG_TMS	I		
	JTAG_TDI	I		
	JTAG_TDO	O		
	SMB_CLK	I/O	SMBus Clock, Open Drain with pull up on ~~platform~~Platform.	1.8 V
	SMB_DATA	I/O	SMBus Data, Open Drain with pull up on ~~platform~~Platform.	1.8 V
	ALERT#	O	Alert notification to master; Open Drain with pull up on ~~platform~~Patform; Active Low.	1.8 V
	DIAG0, DIAG1	I/O	Engineering test mode balls have been specified to allow for special access to DIAG for debug purposes.	

3.4.1. BGA SSD Specific Power and Grounds

In the BGA SSD, there is provision for eight 3.3 V, twelve 1.8 V, twelve 1.2 V, and 104 GND balls. Each ball ~~shall~~ is capable of ~~tolerate~~ tolerating a continuous load of up to 200 mA.

> **Note:** While the maximum current that is possible to be passed to the BGA ~~may be~~is calculated by multiplying the number of power pins by 200 mA, actual power system requirements will be determined between the P~~p~~latform and BGA SSD vendors.

3.4.2. PCI Express Interface

3.4.2.1. PERST#, CLKREQ#, PEWAKE#

Definitions for these signals are the same as that in section 3.1.3, except that these signals are defined to be at signal levels of 1.8 V

See S~~s~~ection 3.3.2~~3.3.2 in this specification~~ for a detailed description of the remaining PCIe signals.

3.4.3. SATA Interface (Informative)

See S~~s~~ection 3.3.3~~, *SATA Interface (Informative)* in this specification~~ for a detailed description of the SATA signals.

3.4.4. SSD Specific Signals

3.4.4.1. SUSCLK

Definition for this signal is the same as that in S~~s~~ection 3.1.11.1,~~3.1.11.1, *UIM POWER SRC* in this specification,~~ except that this signal is defined to be at signal levels of 1.8 V.

3.4.4.2. PEDET

The interface detect ~~can be~~is used by the host computer to determine the communication protocol that the M.2 Adapter ~~module~~ uses; SATA signaling (low) or PCIe signaling (high) in conjunction with a ~~platform~~Platform located pull-up resistor.

3.4.4.3. RFU

Signals documented as RFU are reserved for future use. These balls ~~shall~~ must be soldered to a P~~p~~latform ~~board~~, but ~~shall~~ must be electrically no-connect on the host or the Adapter ~~module~~.

3.4.4.4. ~~DNU (~~DNU~~)~~

Signals documented as Do Not Use (DNU) are for manufacturing only. These balls ~~shall~~ must be soldered to a ~~platform~~ Platform~~board~~, but ~~shall~~ must be electrically no-connect on the host.

3.4.5. SSD Specific Optional Signals

Note: Physical balls need to be present on the package for these signals even if they are not being implemented.

3.4.5.1. CAL_P

This signal is optional and is not required to be connected on the SSD BGA component and is not required to be implemented on the ~~platform~~Platforms ~~boards~~. It is used as impedance reference for controller calibration.

3.4.5.2. RZQ_1 and RZQ_2

These signals are optional and are not required to be connected on the SSD BGA component and are not required to be implemented on the ~~platform~~ Platforms~~boards~~. These signals ~~can be~~are used as impedance reference for calibrating DRAM or NAND memory interface.

3.4.5.3. XTAL_OUT

This signal is optional and is not required to be connected on the SSD BGA component and is not required to be implemented on the ~~platform~~ Platforms~~boards~~. It connects to optional crystal output from BGA SSD Adapter ~~module~~. Crystal unit characteristics are vendor specific.

3.4.5.4. XTAL_IN

This signal is optional and is not required to be connected on the SSD BGA component and is not required to be implemented on the ~~platform~~ Platforms~~boards~~. It connects to optional crystal output from the ~~platform~~Platform. Crystal unit characteristics are vendor specific.

3.4.5.5. JTAG Signals

This group of signals is optional. It is not required to be connected on the SSD BGA component and is not required to be implemented on ~~the~~ the P~~p~~latforms ~~boards~~. IEEE Standard 1149.1 specifies the rules and permissions for designing an 1149.1-compliant interface. Inclusion of a *Test Access Port* (TAP) on an Adapter ~~module~~ allows boundary scan to be used for testing of the Adapter ~~module~~ on which it is installed. The TAP is comprised of five signals (the JTAG_TRST# signal is optional within the set of JTAG signals) that are used to interface serially with a TAP controller within the BGA based SSD device. The Adapter ~~module~~ vendor must specify TDO drive strength.

3.4.5.6. SMBus Pins

ALERT#, SMB_DATA and SMB_CLK signals are optional and are not required to be connected on the SSD BGA component and are not required to be implemented on the P~~p~~latforms~~ boards~~.

3.4.5.6.1. ALERT#

For a description of this signal, see S~~s~~ection 3.2.12.2.1.

3.4.5.6.2. SMB_DATA

For a description of this signal, see S~~s~~ection 3.2.12.2.2.

3.4.5.6.3. SMB_CLK

For a description of this signal, see S~~s~~ection 3.2.12.2.3.

3.4.5.7. DIAG0, DIAG1

The DIAG0 and DIAG1 signals are optional for engineering or production implementation, are not required to be present on the SSD BGA component, and are not required to be implemented on the ~~platform~~Platforms~~ boards~~.

3.4.6. BGA SSD Soldered-Down Module ~~Module~~ Pin-out

All pinout tables in this section are written from the Module ~~module~~ point of view when referencing signal directions. This section contains the Module~~module~~-side pinout map for Type 1620 BGA Module ~~module~~.

Figure 104 shows Module~~module~~-side ballmap for Type 1620 BGA. Figure 105 shows Type 1620 BGA Module~~module~~-side ballmap surrounded by Type 2024, Type 2228, and Type 2828 module-side ballmaps (Top View).

There are additional sizes of 2024, 2228, and 2828 defined for BGA SSD. Ballmaps for these sizes encompass the Type 1620 ballmap with additional DNU balls for mechanical stability. See section 2.3.6, Soldered-Down Form Factors for BGA SSDs for details on the location of these DNU balls for various BGA package sizes.

Optional signals are shown in blue. The optional signals are CAL_P, XTAL_OUT, XTAL_IN, RZQ_1, RZQ_2, DIAG0, DIAG1, JTAG_TRST#, JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO, SMB_CLK, SMB_DATA, and ALERT#.

The optional signals are handled as follows for the host and Module ~~module~~.

- Host:
  - If not implemented, the landing pads ~~shall~~ must not be electrically connected to the host.
  - If implemented, the host routes the signals as described in this specification.
- Module
  - If not implemented, the balls ~~shall~~ must not be electrically connected to the Module ~~module~~.
  - If implemented, the module routes the signals as described in this specification.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
B	DNU	DNU		DNU		CAL_P		DNU			DNU		DNU		DNU		DNU	DNU
C	GND	GND	GND	GND	GND	DNU	XTAL_ OUT	XTAL_IN	DNU	RZQ_1	DNU	DNU	RFU	RFU	GND	DNU	DNU	DNU
D				REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	+3.3 V	+3.3 V	GND	DNU	DIAG1	SUSCLK	RFU			
E	GND	GND	GND	GND	GND	GND	GND	DEVSLP	+3.3 V	+3.3 V	GND	PEWAKE#	DIAG0	GND	GND	DNU	DNU	DNU
F				SATA-A+ / PERp0	SATA-A- /PERn0	GND								PEDET	RFU			
G	GND	GND	GND	GND	GND		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		GND	GND	DNU	DNU	DNU
H				SATA-B+ /PETp0	SATA-B- /PETn0		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		RFU	RFU			
J	GND	GND	GND	GND	GND		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		GND	GND	DNU	DNU	DNU
K				PERp1	PERn1		GND	GND	GND	GND	GND	GND		RFU	RFU			
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JTAG_ TRST#
M				PETp1	PETn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU			
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_ TCK	JTAG_ TMS
P				PERp2	PERn2		GND	GND	GND	GND	GND	GND		RFU	RFU			
R	GND	GND	GND	GND	GND		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		GND	GND	DNU	JTAG_ TDI	JTAG_ TDO
T				PETp2	PETn2		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		RFU	RFU			
U	GND	GND	GND	GND	GND		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		GND	GND	DNU	SMB_ CLK	SMB_ DATA
V				PERp3	PERn3									RFU	RFU			
W	GND	GND	GND	GND	GND	GND	LED1#/ DAS	RFU	+3.3 V	+3.3 V	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#
Y				PETp3	PETn3	GND	DNU	DNU	+3.3 V	+3.3 V	GND	DNU	GND	DNU	DNU			
AA	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	RZQ_2	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU
AB	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
B	DNU	DNU		DNU		CAL_P		DNU			DNU		DNU		DNU		DNU	DNU
C	GND	GND	GND	GND	GND	DNU	XTAL_ OUT	XTAL_IN	DNU	RZQ_1	DNU	DNU	RFU	RFU	GND	DNU	DNU	DNU
D				REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	3.3 V	3.3 V	GND	DNU	DIAG1	SUSCLK	RFU			
E	GND	GND	GND	GND	GND	GND	GND	DEVSLP	3.3 V	3.3 V	GND	PEWAKE#	DIAG0	GND	GND	DNU	DNU	DNU
F				SATA-A+ / PERp0	SATA-A- /PERn0	GND								PEDET	RFU			
G	GND	GND	GND	GND	GND		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		GND	GND	DNU	DNU	DNU
H				SATA-B+ /PETp0	SATA-B- /PETn0		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		RFU	RFU			
J	GND	GND	GND	GND	GND		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		GND	GND	DNU	DNU	DNU
K				PERp1	PERn1		GND	GND	GND	GND	GND	GND		RFU	RFU			
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JTAG_ TRST#
M				PETp1	PETn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU			
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_ TCK	JTAG_ TMS
P				PERp2	PERn2		GND	GND	GND	GND	GND	GND		RFU	RFU			
R	GND	GND	GND	GND	GND		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		GND	GND	DNU	JTAG_ TDI	JTAG_ TDO
T				PETp2	PETn2		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		RFU	RFU			
U	GND	GND	GND	GND	GND		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		GND	GND	DNU	SMB_ CLK	SMB_ DATA
V				PERp3	PERn3									RFU	RFU			
W	GND	GND	GND	GND	GND	GND	LED1#/ DAS	RFU	3.3 V	3.3 V	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#
Y				PETp3	PETn3	GND	DNU	DNU	3.3 V	3.3 V	GND	DNU	GND	DNU	DNU			
AA	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	RZQ_2	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU
AB	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU

= No Solder Ball

Figure 104. Type 1620 BGA Module-side Ballmap (Top View)

Type 2828 →				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
								1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24				
↓	Type 2228 ↓	Type 2024 ↓	Type 1620 → ↓								1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18							
A				DNU	DNU																													DNU	DNU
B	A			DNU				DNU	DNU	DNU	DNU	DNU															DNU	DNU	DNU	DNU	DNU				DNU
C	B	A						DNU	DNU	DNU																			DNU	DNU	DNU				
D	C	B						DNU	DNU																					DNU	DNU				
E	D	C						DNU																							DNU				
F	E	D	A	DNU				DNU			DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU			DNU				DNU
G	F	E	B								DNU	DNU		DNU		CAL_P		DNU			DNU		DNU		DNU		DNU	DNU							
H	G	F	C	DNU					DNU		GND	GND	GND	GND	GND	DNU	XTAL_OUT	XTAL_IN	DNU	RZQ_1	DNU	DNU	RFU	RFU	GND	DNU	DNU	DNU		DNU					DNU
J	H	G	D											REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	+3.3 V	+3.3 V	GND	DNU	DIAG1	SUSCLK	RFU										
K	J	H	E	DNU				DNU			GND	GND	GND	GND	GND	GND	GND	DEVSLP	+3.3 V	+3.3 V	GND	PEWAKE#	DIAG0	GND	GND	DNU	DNU	DNU			DNU				DNU
L	K	J	F											SATA-A+/PERp0	SATA-A-/PERn0	GND								PEDET	RFU										
M	L	K	G	DNU				DNU			GND	GND	GND	GND	GND		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		GND	GND	DNU	DNU	DNU			DNU				DNU
N	M	L	H											SATA-B+/PETp0	SATA-B-/PETn0		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		RFU	RFU										
P	N	M	J					DNU			GND	GND	GND	GND	GND		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		GND	GND	DNU	DNU	DNU			DNU				
R	P	N	K											PERp1	PERn1		GND	GND	GND	GND	GND	GND		RFU	RFU										
T	R	P	L					DNU			GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JTAG_TRST#			DNU				
U	T	R	M											PETp1	PETn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU										
V	U	T	N					DNU			GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_TCK	JTAG_TMS			DNU				
W	V	U	P											PERp2	PERn2		GND	GND	GND	GND	GND	GND		RFU	RFU										
Y	W	V	R					DNU			GND	GND	GND	GND	GND		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		GND	GND	DNU	JTAG_TDI	JTAG_TDO			DNU				
AA	Y	W	T											PETp2	PETn2		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		RFU	RFU										
AB	AA	Y	U	DNU				DNU			GND	GND	GND	GND	GND		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		GND	GND	DNU	SMB_CLK	SMB_DATA			DNU				DNU
AC	AB	AA	V											PERp3	PERn3									RFU	RFU										
AD	AC	AB	W	DNU				DNU			GND	GND	GND	GND	GND	GND	LED1#/ DAS	RFU	+3.3 V	+3.3 V	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#			DNU				DNU
AE	AD	AC	Y											PETp3	PETn3	GND	DNU	DNU	+3.3 V	+3.3 V	GND	DNU	GND	DNU	DNU										
AF	AE	AD	AA	DNU					DNU		GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	RZQ_2	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU		DNU					DNU
AG	AF	AE	AB								DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU							
AH	AG	AF	AC	DNU				DNU			DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU			DNU				DNU
AJ	AH	AG						DNU																							DNU				
AK	AJ	AH						DNU	DNU																					DNU	DNU				
AL	AK	AJ						DNU	DNU	DNU																			DNU	DNU	DNU				
AM	AL			DNU				DNU	DNU	DNU	DNU	DNU															DNU	DNU	DNU	DNU	DNU				DNU
AN				DNU	DNU																													DNU	DNU

2125

Type 2828				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
	Type 2228							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24				
		Type 2024	Type 1620								1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18							
A				DNU	DNU																													DNU	DNU
B	A			DNU				DNU	DNU	DNU	DNU	DNU															DNU	DNU	DNU	DNU	DNU				DNU
C	B	A						DNU	DNU	DNU																			DNU	DNU	DNU				
D	C	B						DNU	DNU																					DNU	DNU				
E	D	C						DNU																							DNU				
F	E	D	A	DNU				DNU			DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU			DNU				DNU
G	F	E	B								DNU	DNU		DNU		CAL_P		DNU			DNU		DNU		DNU		DNU	DNU							
H	G	F	C	DNU					DNU		GND	GND	GND	GND	GND	DNU	XTAL_OUT	XTAL_IN	DNU	RZQ_1	DNU	DNU	RFU	RFU	GND	DNU	DNU	DNU		DNU					DNU
J	H	G	D											REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	3.3 V	3.3 V	GND	DNU	DIAG1	SUSCLK	RFU										
K	J	H	E	DNU				DNU			GND	GND	GND	GND	GND	GND	GND	DEVSLP	3.3 V	3.3 V	GND	PEWAKE#	DIAG0	GND	GND	DNU	DNU	DNU			DNU				DNU
L	K	J	F											SATA-A+ /PERp0	SATA-A- /PERn0	GND								PEDET	RFU										
M	L	K	G	DNU				DNU			GND	GND	GND	GND	GND		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		GND	GND	DNU	DNU	DNU			DNU				DNU
N	M	L	H											SATA-B+ /PETp0	SATA-B- /PETn0		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		RFU	RFU										
P	N	M	J					DNU			GND	GND	GND	GND	GND		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		GND	GND	DNU	DNU	DNU			DNU				
R	P	N	K											PERp1	PERn1		GND	GND	GND	GND	GND	GND		RFU	RFU										
T	R	P	L					DNU			GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JTAG_TRST#			DNU				
U	T	R	M											PETp1	PETn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU										
V	U	T	N					DNU			GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_TCK	JTAG_TMS			DNU				
W	V	U	P											PERp2	PERn2		GND	GND	GND	GND	GND	GND		RFU	RFU										
Y	W	V	R					DNU			GND	GND	GND	GND	GND		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		GND	GND	DNU	JTAG_TDI	JTAG_TDO			DNU				
AA	Y	W	T											PETp2	PETn2		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		RFU	RFU										
AB	AA	Y	U	DNU				DNU			GND	GND	GND	GND	GND		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		GND	GND	DNU	SMB_CLK	SMB_DATA			DNU				DNU
AC	AB	AA	V											PERp3	PERn3									RFU	RFU										
AD	AC	AB	W	DNU				DNU			GND	GND	GND	GND	GND	GND	LED1#/ DAS	RFU	3.3 V	3.3 V	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#			DNU				DNU
AE	AD	AC	Y											PETp3	PETn3	GND	DNU	DNU	3.3 V	3.3 V	GND	DNU	GND	DNU	DNU										
AF	AE	AD	AA	DNU					DNU		GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	RZQ_2	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU		DNU					DNU
AG	AF	AE	AB								DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU							
AH	AG	AF	AC	DNU				DNU			DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU			DNU				DNU
AJ	AH	AG						DNU																							DNU				
AK	AJ	AH						DNU	DNU																					DNU	DNU				
AL	AK	AJ						DNU	DNU	DNU																			DNU	DNU	DNU				
AM	AL			DNU				DNU	DNU	DNU	DNU	DNU															DNU	DNU	DNU	DNU	DNU				DNU
AN				DNU	DNU																													DNU	DNU

	Type 1620
	Type 2024
	Type 2228
	Type 2828

Figure 105. Type 1620 BGA Module-side Ballmap Surrounded by Type 2024, Type 2228, and Type 2828 Module-side Ballmaps (Top View)

4

4. Electrical Requirements

CAUTION: M.2 ~~modules~~ Add-in Cards are not designed or intended to support Hot-Swap or Hot-Plug connections. Performing Hot-Swap or Hot-Plug ~~may~~ poses danger to the M.2 ~~module~~Add-in Card, to the system ~~platform~~Platform, and to the person performing this act.

4.1. 3.3 V Logic Signal Requirements

The 3.3 V card logic levels for single-ended digital signals (PEWAKE#, CLKREQ#, PERST#, SUSCLK, W_DISABLE#, UART_WAKE, DP_MLDIR, LED#) are given in Table 40. When used in the BGA SSD applications, the logic levels for WAKE#, CLKREQ#, PERST#, and SUSCLK are those shown in Table 41.

Table 40. DC Specification for 3.3 V Logic Signaling

Symbol	Parameter	Condition	Min	Max	Unit	Notes
~~+~~3.3 V	Supply Voltage		3.135	3.465	V	
V_{IH}	Input High Voltage		2.0	3.6	V	5
V_{IL}	Input Low Voltage		-0.5	0.8	V	5
I_{OL} ~~L~~	Output Low Current for open-drain signals	0.4 V	4		mA	1
I_{OH} ~~L~~	Output ~~Low~~ High Current for open-drain signals	0.4 V	9		mA	2
I_{IN}	Input Leakage Current	0 V to 3.3 V	-10	+10	μA	5
I_{LKG}	Output Leakage Current	0 V to 3.3 V	-50	+50	μA	5
C_{IN}	Input Pin Capacitance			7	pF	5
C_{OUT}	Output Pin Capacitance			30	pF	4
$R_{PULL-UP}$	Pull-up Resistance		9	60	kΩ	3

Notes: 1. Not applicable to LED# and DAS/DSS# pins.
2. Applies to the LED# pins.
3. Applies to CLKREQ# and PEWAKE# pull-up on host system.
4. As measured at the card connector pad.

5. Applies to PERST#, W_DISABLE1#, W_DISABLE2#, MLDIR (when applicable) and PEWAKE# (when used for OBFF signaling).

4.2. 1.8 V Logic Signal Requirements

The 1.8 V card logic levels for single-ended digital signals (SDIO, UART, I2C, PCM/I2S, SMBus, etc.) are given in Table 41. This table also defines the signaling levels for BGA SSD defined single-ended signals such as (PERST#, CLKREQ#, PEWAKE#, SUSCLK, SMB_CLK, SMB_DAT, ALERT#).

Table 41. DC Specification for 1.8 V Logic Signaling

Symbol	Parameter	Condition	Min	Max	Unit	Notes
V_{DD18}	Supply Voltage		1.7	1.9	V	
V_{IH}	Input High Voltage		0.7*V_{DD18}	V_{DD18}+0.3	V	
V_{IL}	Input Low Voltage		-0.3	0.3*V_{DD18}	V	
V_{OH}	Output High Voltage	I_{OH} = -1mA V_{DD18} Min	V_{DD18}-0.45		V	
V_{OL}	Output Low Voltage	I_{OL} = 1mA V_{DD18} Min		0.45	V	1
I_{IN}	Input Leakage Current	0 V to V_{DD18}	-10	+10	μA	
I_{LKG}	Output Leakage Current	0 V to V_{DD18}	-50	+50	μA	
C_{IN}	Input Pin Capacitance			10	pF	
$R_{PULL-UP}$	Pull-up Resistance		9	60	kΩ	2

Note 1: The listed I_{OL} may not meet some SMBus designs and an isolation buffer may be required. Refer to the *SMBus Specification* for timing and loading details.

2: Applies to CLKREQ# pull-up on host system.

4.3. Electrical Requirements for BGA SSDs

4.3.1. Voltage Supply Power-on Sequencing

The host should apply the following recommendations for sequencing the voltages on the 3.3 V supply, the 1.8 V supply, and the 1.2 V supply during power-on:

- After the voltage on the 1.8 V supply or the voltage on the 1.2 V supply reach 300 mV, the voltage on the 1.8 V supply should remain greater than the voltage on the 1.2 V supply by at least 200 mV.
- The voltage on the 3.3 V supply has no timing relationship relative to the voltage on the 1.2 V supply or the voltage on the 1.8 V supply.

If the power-on sequencing recommendations are not followed, there is a risk that the device may not power-on correctly or the device may be damaged. These results are vendor specific, and the implications may not be seen immediately.

Figure 106 shows three valid power-on ramp examples.

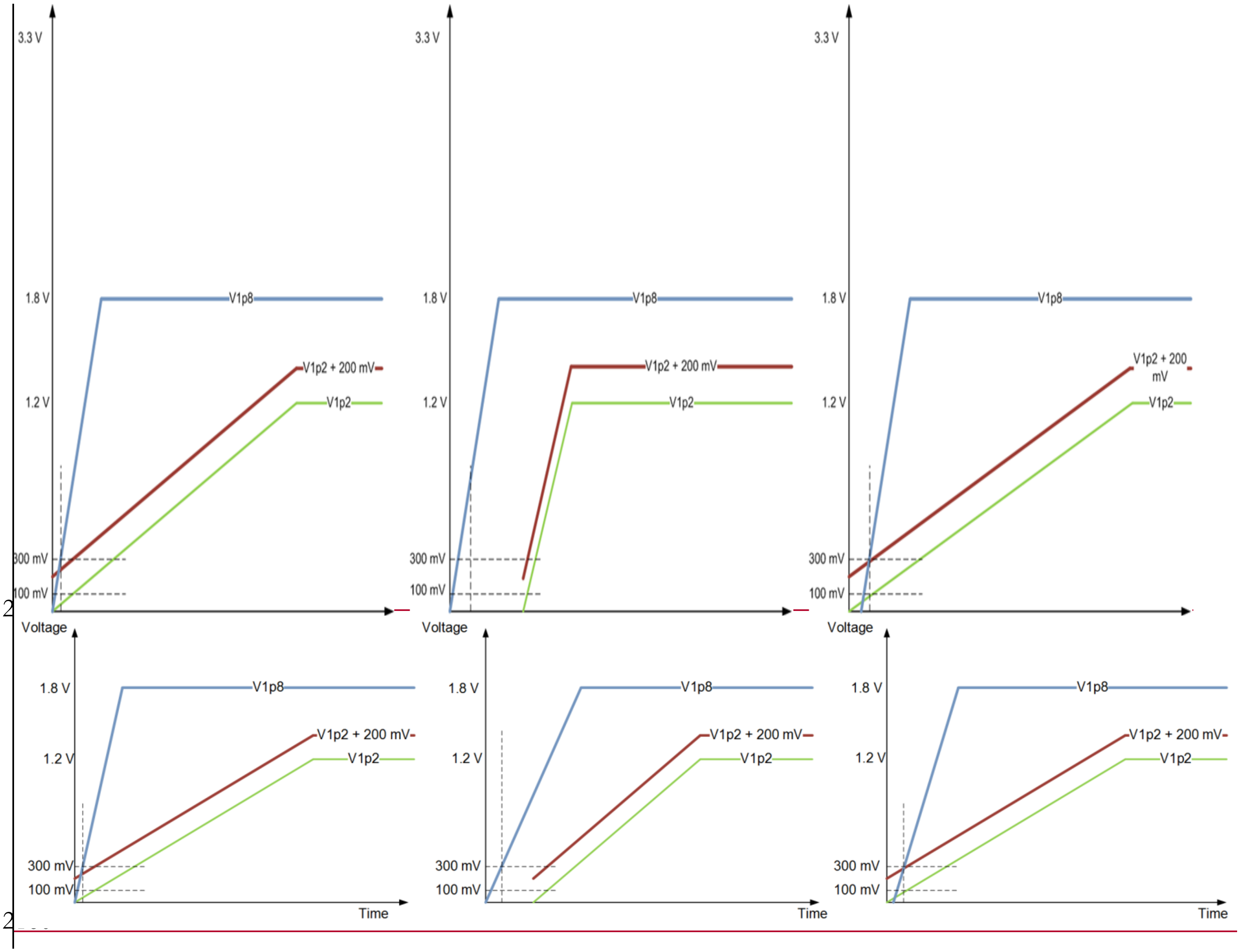


Figure 106. Power-on Sequencing

4.3.2. Voltage Supply Power-off Sequencing

The host should apply the following recommendations for sequencing the voltages on the 3.3 V supply, the 1.8 V supply, and the 1.2 V supply during power-off:

- Before the voltage on the 1.2 V supply and the voltage on the 1.8 V supply reach 300 mV, the voltage on the 1.8 V supply should remain greater than voltage on the 1.2 V supply by 200 mV.
- After both the voltage on the 1.8 V supply and the voltage on the 1.2 V supply are below 300 mV, there is no specified relationship between them.

- The voltage on the 3.3 V supply has no timing relationship relative to the voltage on the 1.2 V supply or the voltage on the 1.8 V supply.
- The voltage on all supplies ~~should~~ must remain below 100 mV for at least 1 ms before the power-on sequence is restarted.

If the power-off sequencing recommendations are not followed, there is a risk that the device may not power-on correctly or the device may be damaged. These results are vendor specific, and the implications may not be seen immediately.

Figure 107 shows two valid power-off ramp examples.

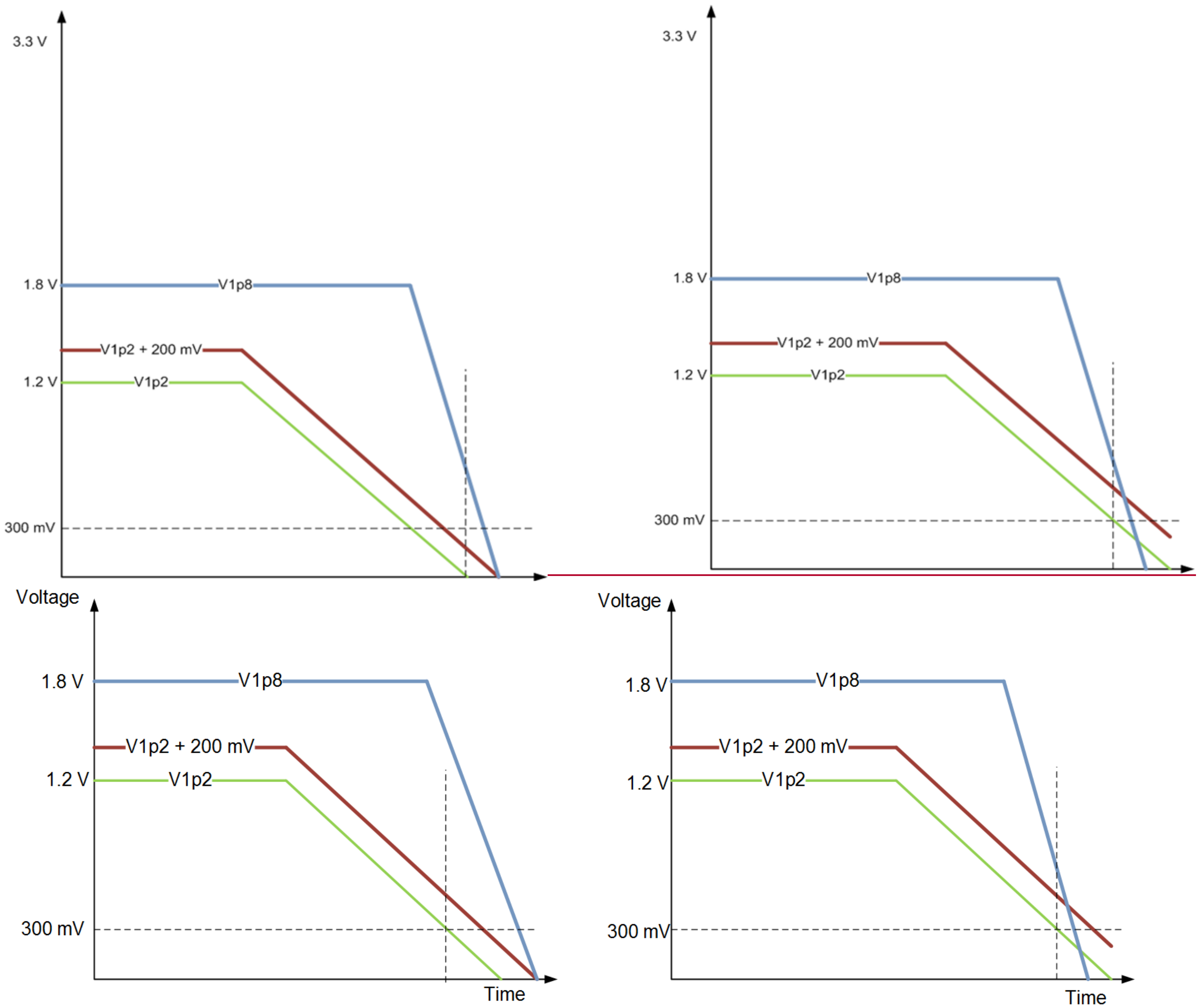


Figure 107. Power-off Sequence

4.3.3. Power Ramp Timing

The power ramp timing is defined as the time the power rail needs to ramp to a valid voltage (~~shown in~~see Table 42). This timing is recommended for power-on only.

Table 42. Power Ramp Timing

Supply Voltage	Max*
3.3 V	35 ms
1.8 V	25 ms
1.2 V	20 ms
* The minimum timing may be calculated from the maximum slew rate recommendation in Table 43.	

4.3.4. Power Rail Slew Rate

The maximum power rail slew rate is shown in Table 43. These values are only defined for ESD protection purpose. They are not meant for inrush current control.

Table 43. Power Rail Slew Rate

Symbol	Parameter	Max	Condition
$T_{SLEW\_3.3}$	Voltage slew rate of the 3.3 V power rail	100 kV/s	No Load
$T_{SLEW\_1.8}$	Voltage slew rate of the 1.8 V power rail	100 kV/s	No Load
$T_{SLEW\_1.2}$	Voltage slew rate of the 1.2 V power rail	100 kV/s	No Load

4.4. Power

The M.2 Adapter utilizes a single regulated power rail of 3.3 V provided by the P~~p~~latform. In some pinout Adapter~~variants~~, there is a dedicated VIO supply pin called VIO1.8V that is intended to only bias the I/O circuitry of the ~~module~~Adapter. The main 3.3 V and the VIO voltage rail sources on the ~~platform~~ Platform should always be on and available during the system's stand-by/suspend state to support the wake event processing on the communications card. Some NICs ~~may~~ require host (driver) intervention after a power-on.

The number of 3.3 V pins for any given pinout is determined by the maximum required instantaneous current typical of the solutions associated with each type of socket and the M.2 connector current handling capability per pin. The M.2 connector pin is defined as needing to support 500 mA/pin continuous. This yields the required number of power rail pins per pinout.

- Type 1630, intended for Socket 1, has two power pins allocated in the pinouts that supports up to 1 A continuous.
- Types 2230 and 3030, intended for Socket 1, have four power pins in their pinouts and ~~can~~ support up to 2 A continuous.
- The Socket 2 board types have five power pins in their pinouts and support up to 2.5 A continuous.
- The Socket 3 board types, with a single ~~Module~~ Add-in Card Key, have nine power pins but ~~can~~ support
  up to 2.5 A continuous.
- The four extra power pins enable reduced IR drop for these devices.

The power rail voltage tolerance listed in Table 44 is ±5% for 3.3 V rail. This is different from the ± 9% tolerance allowed in the *PCI Express Mini Card S~~s~~pecification*.

Table 44. Key Regulated Power Rail Parameters

Power Rail	Pin Name	Voltage Tolerance	~~Platform~~Platform Rail Type
~~+~~3.3 V	3.3 V	±5%	Always On
~~+~~1.8 V	VIO1.8 V	±5.55%*	Always On
~~+~~1.2 V	1.2 V	±5%	Always On
~~+~~1.8 V	1.8 V	±5.55%	Always On
Note*: 1.7 V to 1.9 V Range			

Alternatively, and primarily for ~~Tablet~~ Tablet P~~p~~latforms, the 3.3 V regulated power rail ~~can be~~is permitted to be replaced with a direct V_{BAT} connection. In such a case, the ~~module~~ Adapter will need to produce any and all required voltages needed to support those Adapters ~~modules~~ and meet the ~~Host I/F~~host interface voltage levels defined in section 3.2. The current limit per pin of 500 mA/pin would still apply even if connected to V_{BAT}. Note that the requirements in Table 45 only apply to Socket 2 WWAN-based Adapter ~~module~~ pinouts.~~:~~

Table 45. Key V_{BAT} Power Rail Parameters

Power Source	V_{MIN}	V_{MAX}	Cell Type
V_{BAT}	3.135 V	4.4 V	One cell Li-ion battery

The power rating of each M.2 Adapter ~~module~~ type is different based on the technology that is enabled and defined by the M.2 connector key. A list of connector keys and the power rating enabled for those keys is given in Table 46.

Table 46. Power Rating Table for M.2 ~~Modules~~ Add-in Cards

Key	Power Rail	Voltage Tolerance	Current Consumption Limit	
			Peak mA Max Avg @ 100 µs	**Normal mA** Max Avg @ 1 s
A	3.3 V	± 5%	2000	
B	3.3 V	± 5%	2500	
B	V_{BAT}	3.135 V – 4.4 V	2500	
C	3.3 V	± 5%	2500	
C	V_{BAT}	3.135 V – 4.4 V	2500	
C	1.8 V (see Note 1)	± 5.55% (see Note 2)	70	
D	RFU	RFU	RFU	RFU
E	3.3 V	± 5%	2000	
F	RFU	RFU	RFU	RFU
G	N/A	N/A	N/A	N/A
H	RFU	RFU	RFU	RFU
J	RFU	RFU	RFU	RFU
K	RFU	RFU	RFU	RFU
L	RFU	RFU	RFU	RFU
M	3.3 V	± 5%	2500	

Notes:

Peak The maximum highest averaged current value over any 100 µs period
Normal The maximum highest averaged current value over any 1 s period

1. Pin name VIO1.8V
2. 1.7 V to 1.9 V Range

The operation of the 3.3 V power source must conform to the *PCI Bus Power Management Interface Specification* and the *Advanced Configuration and Power Interface (ACPI) Specification*, except as otherwise specified by this document.

5. ~~Platform~~Platform Socket Pinout and Key Definitions

> All pinouts tables in this section are written from the ~~Platform~~Platform point of view when referencing signal directions.

In all pinouts, the Power Rail referred to in the M.2 connectors are the 3.3 V rail unless otherwise indicated.

The M.2 pinouts are primarily intended to allocate specific pin functionalities that need to be routed on the ~~Platform~~Platform side to the respective Edge Card Slot Connector. Although many Host I/Fs are supported in the various pinouts, it does not necessarily imply that all I/F needs to be supported by the ~~Add-In card/module~~Adapter at the same time. But the assigned allocations will enable each vendor and ~~Platform~~Platform to design their circuits with the aligned pin assignment.

In some cases, multiple Host I/Fs and other signals are overlaid using the same pin assignment. In these cases, there are sense pins that clearly identify what assignment is supported by the Adapter ~~Add-In card~~ so that automatic multiplexing/routing would be possible on the P~~p~~latform.

A mechanical connector key/~~module~~ Add-in Card key scheme is introduced to distinguish between different pinouts and functionalities because of the various connectorized pinout assignments needed in support of the multiple add-in functions and to prevent wrongful insertions. However, all these connectors share the same basic connection scheme of a Gold Finger Edge Card that plugs into a slot connector mounted on the ~~platform~~ Platform side. Connector mating ~~can only~~ occurs when the Connector Key and Add-in Card ~~Module~~ key align to the same location.

The connector key/Add-in Card ~~module~~ key system used in conjunction with the M.2 75 position connector will enable up to 12 unique key locations and assignments. Different Keys are needed when the family of host interfaces ~~Host I/F~~ differ significantly from each other in support of the different types of Sockets in a ~~platform~~Platform. Connector Keys are associated with the Socket Connector on ~~Platform~~Platform while Add-in Card ~~Module~~ Keys are associated with the Card Edge connection on the Add-in Card ~~Module~~ side.

The initial Key assignments are listed in Table 47. Key ID assignment must be approved by the PCI-SIG. Unauthorized use of Key IDs would render this use as non-compliant to M.2 specifications.

Table 47. Mechanical Key Assignments

Key ID	Pin Location	Key Definition
A	8-15	Display Port Based Connectivity
B	12-19	WWAN/SSD/Others Primary Key
C	16-23	WWAN Key
D	20-27	~~Reserved for Future Use~~RFU
E	24-31	SDIO Based Connectivity
F	28-35	Future Memory Interface
G	39-46	Generic (Not used for M.2)
H	43-50	RFU~~Reserved for Future Use~~
J	47-54	RFU~~Reserved for Future Use~~
K	51-58	RFU~~Reserved for Future Use~~
L	55-62	RFU~~Reserved for Future Use~~
M	59-66	SSD 4 Lane PCIe

~~**Note:** Key ID assignment must be approved by the PCI-SIG. Unauthorized use of Key IDs would render this use as non-compliant to M.2 specifications.~~

5.1. Connectivity Socket; Socket 1

Connectivity Socket 1 will have two Key and Pinouts variations in support of multiple Connectivity Add-In functions (such as Wi-Fi+Bluetooth) along with some additional wireless solutions such as GNSS, NFC, or Wi-Gig. The different Keys will support variations of the functional Host I/Fs as listed in Table 48.

Table 48. Socket 1 Versions

	Socket Version	
	Socket 1 – SDIO Based	Socket 1 – Display Port Based
Mechanical Key	E	A
WiFi	PCIe	
	SDIO	~~(1)~~ (see Note 1)
BT	USB	
	PCM/UART	~~(1)~~ (see Note 1)
WiGig	PCIe	
	~~(1~~) (see Note 1)	DP x4
NFC	I2C (or USB or UART~~(2)~~) (see Note 2)	

~~Module~~ Adapter Types	1630, 2230, 3030	2230, 3030

~~1~~ **Notes:** 1. Not supported
2. Function to host interface ~~Host I/F~~ allocation is a preferred example. Alternative function to host interface ~~Host I/F~~ allocations are possible if using the host interfaces ~~Host I/Fs~~ supported in the pinout and in agreement between Customer ←→ Vendor.

Because several of the interfaces listed in Table 48 have common signals located at the exact same pin locations with only the odd interfaces and mechanical keys trading places, we are able to create ~~modules~~ Adapters with a dual ~~Module~~ Add-in Card Key that ~~can~~ plugs into two different Connector Keys.

5.1.1. Display Port Based Socket 1 (Mechanical Key A) On ~~Platform~~Platform

- Display Port Based Socket 1 pinouts Key A is intended to support Wireless Connectivity devices including combinations of Wi-Fi, BT, NFC, and/or Wi-Gig. Other Combos are possible provided they use the defined Host I/Fs in the pinouts.
- PCIe Lane 0 is intended for use with the Wi-Fi.
- PCIe Lane 1 is intended for use with the Wi-Gig if the PCIe Lane 0 is not shared with the Wi-Fi.
- Four Lane Display Port with assorted sideband signaling is also intended for use with the Wi-Gig.
- LED_1# and W_DISABLE1# are intended for use with the Wi-Fi and Wi-Gig.
- USB and LED_2# are intended for use with the BT. There is only one W_DISABLE# supported by default. ~~However, a~~An adjacent Reserved pin (Pin 54) ~~can be~~is used alternatively as W_DISABLE2# for the BT.
- I2C and ALERT are intended for use with NFC.
- COEX signals are used for coexistence between the different Wireless Comms. Two signals have unique directionality associated with them. All these COEX signals should be connected to the Socket 2 COEX signals for coexistence with the WWAN solution.
- Other Comm/host interface ~~Host I/F~~ combinations are possible. Actual implementation needs to be defined and agreed upon by Vendor←→Customer.

Table 49 provides a list of pin assignments on Socket 1 with mechanical key A.

Table 49. Display Port Based Socket 1 Pinout Diagram (Mechanical Key A) On ~~Platform~~Platform

Pin	Signal	Signal	Pin
		GND	75
74	3.3 V	REFCLKn1	73
72	3.3 V	REFCLKp1	71
70	PEWAKE1# (I/O)(0/3.3V)	GND	69
68	CLKREQ1# (I/O)(0/3.3V)	PERn1	67
66	PERST1# (O)(0/3.3V)	PERp1	65
64	RESERVED	GND	63
62	ALERT# (I)(0/1.8 V)	PETn1	61
60	I2C_CLK (O)(0/1.8 V)	PETn1	59
58	I2C_DATA (I/O)(0/1.8 V)	GND	57
56	W_DISABLE1# (O)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
54	W_DISABLE2# (O)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
52	PERST0# (O)(0/3.3V)	GND	51
50	SUSCLK(32kHz) (O)(0/3.3V)	REFCLKn0	49
48	COEX_TXD (O)(0/1.8V)	REFCLKp0	47
46	COEX_RXD (I)(0/1.8V)	GND	45
44	COEX3 (I/O)(0/1.8V)	PERn0	43
42	VENDOR DEFINED	PERp0	41
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PETn0	37
36	GND	PETp0	35
34	DP_ML0p	GND	33
32	DP_ML0n	DP_HPD (I/O)(0/3.3V)	31
30	GND	GND	29
28	DP_ML1p	DP_ML2p	27
26	DP_ML1n	DP_ML2n	25
24	GND	GND	23
22	DP_AUXp	DP_ML3p	21
20	DP_AUXn	DP_ML3n	19
18	GND	MLDIR Sense (I)	17
16	LED_2# (I)(OD)	CONNECTOR KEY A	
	CONNECTOR KEY A	CONNECTOR KEY A	
	CONNECTOR KEY A	CONNECTOR KEY A	
	CONNECTOR KEY A	CONNECTOR KEY A	
	CONNECTOR KEY A	GND	7
6	LED_1# (I)(OD)	USB_D-	5
4	3.3 V	USB_D+	3
2	3.3 V	GND	1

5.1.2. SDIO Based Socket 1 (Mechanical Key E) On ~~Platform~~Platform

- SDIO Based Socket 1 pinouts Key E is intended to support Wireless Connectivity devices including combinations of Wi-Fi, BT, NFC, and/or GNSS. Other Combos are possible provided they use the defined Host I/Fs.
- PCIe Lane 0 or SDIO, LED_1#, and W_DISABLE1# are intended for use with Wi-Fi.
- USB or UART+PCM, LED_2# is intended for use with BT. There is only one W_DISABLE# supported by default.~~ However, ~~ ~~a~~An adjacent Reserved pin (Pin 54) ~~can be~~is used alternatively as W_DISABLE2# for the BT.
- PCIe Lane 1 PET and PER are intended for future expansion in case a two Lane PCIe is needed (~~for example,. with Wi-Gig Combo).~~
- ~~I2C and~~e.g., with Wi-Gig Combo).
- I2C and ALERT# are intended for use with NFC.
- COEX signals are used for coexistence between the different Wireless Comms. Two signals have unique directionality associated with them. All these COEX signals should be connected to Socket 2 COEX signals for coexistence with the WWAN solution.
- Other Comm or ~~/~~host interface ~~Host I/F~~ combinations are possible. Actual implementation needs to be defined and agreed upon by Vendor←→Customer.

The pin assignments on SDIO based socket 1 with mechanical key E are given in Table 50.

Table 50. SDIO Based Socket 1 Pinout Diagram (Mechanical Key E) On ~~Platform~~Platform

Pin	Signal	Signal	Pin
74	3.3 V	GND	75
72	3.3 V	RESERVED/REFCLKn1	73
70	UIM_POWER_SRC/GPIO_1/PEWAKE1#	RESERVED/REFCLKp1	71
68	UIM_POWER_SNK/CLKREQ1#	GND	69
66	UIM_SWP/PERST1#	RESERVED/PERn1	67
64	RESERVED	RESERVED/PERp1	65
62	ALERT# (I)(0/1.8 V)	GND	63
60	I2C_CLK (O)(0/1.8 V)	RESERVED/PETn1	61
58	I2C_DATA (I/O)(0/1.8 V)	RESERVED/PETp1	59
56	W_DISABLE1# (O)(0/3.3V)	GND	57
54	W_DISABLE2# (O)(0/3.3V)	PEWAKE0# (I/O)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
50	SUSCLK(32kHz) (O)(0/3.3V)	GND	51
48	COEX_TXD (O)(0/1.8V)	REFCLKn0	49
46	COEX_RXD (I)(0/1.8V)	REFCLKp0	47
44	COEX3 (I/O)(0/1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	UART RTS (O)(0/1.8V)	PETn0	37
34	UART CTS (I)(0/1.8V)	PETp0	35
32	UART TXD (O)(0/1.8V)	GND	33
	CONNECTOR Key E	CONNECTOR KEY E	
	CONNECTOR Key E	CONNECTOR KEY E	
	CONNECTOR KEY E	CONNECTOR KEY E	
	CONNECTOR KEY E	CONNECTOR KEY E	
22	UART RXD (I)(0/1.8V)	SDIO RESET#/TX_BLANKING (O)(0/1.8V)	23
20	UART WAKE# (I)(0/3.3V)	SDIO WAKE# (I)(0/1.8V)	21
18	GND	SDIO DATA3(I/O)(0/1.8V)	19
16	LED_2# (I)(OD)	SDIO DATA2(I/O)(0/1.8V)	17
14	PCM_OUT/I2S SD_OUT (O)(0/1.8V)	SDIO DATA1(I/O)(0/1.8V)	15
12	PCM_IN/I2S SD_IN (I)(0/1.8V)	SDIO DATA0(I/O)(0/1.8V)	13
10	PCM_SYNC/I2S WS (I/O)(0/1.8V)	SDIO CMD(I/O)(0/1.8V)	11
8	PCM_CLK/I2S SCK (I/O)(0/1.8V)	SDIO CLK/SYSCLK (O)(0/1.8V)	9
6	LED_1# (I)(OD)	GND	7
4	3.3 V	USB_D-	5
2	3.3 V	USB_D+	3
		GND	1

5.1.3. Dual ~~Module~~ Key ~~Module~~Add-in Card: Supports SDIO Based Socket 1 and Display Port Based Socket 1

In cases where the Connectivity type solutions adopt the Dual ~~Module~~ Add-in Card Key scheme, where the solution use only PCIe, USB, and I2C host interfaces, they ~~can be~~are capable of being inserted into ~~the~~ both SDIO based Socket 1 and Display Port based Socket 1.

See Table 24 for an example of an Add-in Card ~~Module~~-side pinouts that makes use of the Dual Add-in Card ~~Module~~ Key option.

5.2. WWAN+GNSS/SSD/Other Socket; Socket 2

Socket 2 supports various WWAN+GNSS (Global Navigation Satellite System that ~~may~~ includes GPS, GLONASS, and/or Galileo), SSD, and other functional ~~add-in cards~~Adapters. Key B supports different types of functional ~~add-in cards~~Adapters while Key C is primarily targeting WWAN+GNSS functional Adapters~~add-in cards~~. In Key B, this is done by ~~Overlaying~~ overlaying functional pins that ~~can be~~are identified with the aid of Configuration pins and/or having functional pins at different pin allocations in the pinout. In Key C, this is done by overlaying functional pins that are set/defined in a specific implementation in a BTO/CTO agreement between customer and vendor.

Socket 2 is primarily targeted for board types 2230, 2242, 3042, 2260, 2280, and 22110 board sizes. See Table 1 in this specification for board sizes associated with different functional Adapter ~~add-in card~~ types.

5.2.1. Socket 2 Key B

5.2.1.1. Socket 2 Key B – Configuration Pin Definitions

The Socket 2 Key (Mechanical Key B) is unique in that it enables five major pinouts configurations and four variants for each of the three WWAN configurations. The five major configurations supported are:

- WWAN that is PCIe Based
- WWAN that is SSIC Based
- WWAN that is USB3.1 Gen1 Based
- SSD that is PCIe (2 lane) Based
- SSD that is SATA Based

All Socket 2 WWAN pinouts configurations (1, 2, and 3) support USB2.0 and USB HS with the generic USB_D± pins as a baseline. All three have four alternate functional pins, with the aid of twelve GPIO pin allocations, in support of various secondary functions such as GNSS interface and coexistence pins, second UIM support, Audio support, and ~~Reserved for Future Use~~RFU pins.

The ~~Platform~~Platform must read all four Configuration pins so it ~~can~~ clearly identifies~~y~~ which unique configurations needed to be supported. The Platform is capable of~~platform canalso~~ identifying~~y~~ when no ~~module~~ Add-in Card is plugged into the slot.

It is mandatory that the Add-in Card ~~Module~~ side maintain the Configuration Pin states correctly to enable interoperability between the systems that make use and do not make use of these Configuration Pins.

The configuration pins are:

- Pin 21 – CONFIG_0
- Pin 69 – CONFIG_1
- Pin 75 – CONFIG_2
- Pin 1 – CONFIG_3

For the ~~Platform~~Platform to read these Configuration bits, it must pull-up these four pins to an appropriate power rail. If designed properly, the Platform is capable of reading these configuration bits ~~these configuration bits can be read~~ even if the Add-in Card ~~Module~~ is not powered up.

Table 51 shows all the variant configurations as a function of the configuration bits. The ~~Platform~~Platform ~~can then~~ adjusts its host interface connection and supports signal connections to the proper setting to work with the Add-in Card~~Module~~.

Table 51. Socket 2 Add-in Card ~~Module~~ Configuration Table

Add-in Card ~~Module~~ Configuration Decodes				Add-in Card ~~Module~~ Type and Main Host Interface (see Note 1)	Port Configuration (see Note 2)
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)		
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A
0	0	1	0	WWAN – PCIe	0
0	1	1	0	WWAN – PCIe	1
0	0	0	1	WWAN - USB3.1 Gen1	0
0	1	0	1	WWAN - USB3.1 Gen1	1
0	0	1	1	WWAN - USB3.1 Gen1	2
0	1	1	1	WWAN - USB3.1 Gen1	3
1	0	0	0	WWAN - SSIC	0
1	1	0	0	WWAN - SSIC	1
1	0	1	0	WWAN - SSIC	2
1	1	1	0	WWAN - SSIC	3
1	0	0	1	WWAN - PCIe	2
1	1	0	1	WWAN - PCIe	3

1	0	1	1	RFU	N/A
1	1	1	1	No Add-in Card ~~Module~~ Present	N/A

Notes:
1. USB 2.0 supported on all WWAN configurations (HSIC supported on WWAN configuration 3).
2. Applicable to WWAN only.

The four configuration pins listed in Table 51 need to be set to ~~Not Connected (~~NC~~)~~ or ~~Ground (~~GND~~)~~ on the Add-In ~~Module~~ Card side as listed in Table 26. By sensing and decoding these pins the ~~Platform~~Platform ~~can~~ configures the pinout configuration and functionality.

5.2.1.2. Socket 2 Pinout (Mechanical Key B) On ~~Platform~~Platform

- Socket 2 pinouts is intended to support WWAN+GNSS, SSD, and Other types of Add-In solutions with the defined and configurable Host I/Fs.
- WWAN ~~can~~ makes use of USB2.0, USB3.1 Gen1, PCIe (up to two Lanes), or SSIC host I/Fs. The actual implemented I/F is identified through the Configuration pins state (1 of 16 states) on the Add-in Card ~~Module~~ side. LED_1# and W_DISABLE1# are intended for use with the WWAN solution. There are additional WWAN and GNSS related pins including W_DISABLE2#, DPR, and WAKE_ON_WWAN#.
- The UIM and SIM Detect pins are used in conjunction with a SIM device in support of the WWAN solution.
- COEX signals are used for coexistence between the different Wireless Comms. Two signals have unique directionality associated with them. All these COEX signals should be connected to Socket 1 COEX signals for coexistence with the Connectivity solution.
- The ANTCTL pins are placeholders for future expansion and definition of these functions.
- The GPIO_~~[~~0~~…~~ to GPIO_11~~]~~ pins are configurable with four different variants. These variants ~~can be in~~ support ~~of~~ the GNSS interface, second UIM/SIM, Audio interfaces, HSIC and IPC sidebands. The exact definition is determined by which configuration was identified by decoding the four Configuration pins.
- The FULL_CARD_POWER_OFF# and the RESET# pins are unique and intended to be used when the WWAN solution is plugged into ~~Platform~~Platforms that provide a direct connection to VBA~~T~~T (and not a regulated 3.3 V) such as Tablet ~~Platform~~Platforms. They are not used in NB and v~~V~~ery thin notebooks type ~~Platform~~Platforms that provide a regulated 3.3 V power rail. But the FULL_CARD_POWER_OFF# signals should be tied to the 3.3 V power rail on the NB/very thin ~~Platform~~Platform.
- The SSD ~~can~~ makes use of the PCIe two Lanes or overlaid SATA host interface~~host I/F~~. The actual implemented I/F is identified through the CONFIG_1 pin state (1 or 0) in conjunction with the other three Configuration pin states that are all 0. DAS/DS~~S~~S# (overlaid on the LED_1#) and DEVSLP are intended for use with the SATA SSD solution. The SMBus interface ~~may be~~is used by host as side band management interface for SSD configuration, monitoring SSD status, and other diagnostic purposes.

- The SUSCLK pin provides a Slow Clock signal of 32 kHz to enable Low Power States.
- Pins labeled NC should Not Be Connected.

Table 52 lists the pinouts for Socket 2 (mechanical key B).

Table 52. Socket 2 Pinouts Diagram (Mechanical Key B) On ~~Platform~~Platform

Pin	Signal	Signal	Pin
		CONFIG_2	75
74	3.3 V	GND	73
72	3.3 V	GND	71
70	3.3 V	CONFIG_1	69
68	SUSCLK(32kHz) (O)(0/3.3V)	RESET# (O)(0/1.8V)	67
66	SIM DETECT (O)	ANTCTL3 (I)(0/1.8V)	65
64	COEX_RXD (I)(0/1.8V)	ANTCTL2 (I)(0/1.8V)	63
62	COEX_TXD (O)(0/1.8V)	ANTCTL1 (I)(0/1.8V)	61
60	COEX3 (I/O)(0/1.8V)	ANTCTL0 (I)(0/1.8V)	59
58	NC	GND	57
56	NC	REFCLKp	55
54	PEWAKE# (I/O)(0/3.3V)	REFCLKn	53
52	CLKREQ# (I/O)(0/3.3V)	GND	51
50	PERST# (O)(0/3.3V)	PETp0/SATA-A+	49
48	GPIO_4 (I/O)(0/1.8V)	PETn0/SATA-A-	47
46	GPIO_3 (I/O)(0/1.8V)	GND	45
44	GPIO_2 (I/O)/ALERT# (I)/(0/1.8V)	PERp0/SATA-B-	43
42	GPIO_1 (I/O)/SMB_DATA (I/O)/(0/1.8V)	PERn0/SATA-B+	41
40	GPIO_0 (I/O)/SMB_CLK (I/O)/(0/1.8V)	GND	39
38	DEVSLP (O)	PETp1/USB3.1-Tx+/SSIC-TxP	37
36	UIM-PWR (I)	PETn1/USB3.1-Tx-/SSIC-TxN	35
34	UIM-DATA (I/O)	GND	33
32	UIM-CLK (I)	PERp1/USB3.1-Rx+/SSIC-RxP	31
30	UIM-RESET (I)	PERn1/USB3.1-Rx-/SSIC-RxN	29
28	GPIO_8 (I/O) (0/1.8V)	GND	27
26	GPIO_10 (I/O) (0/1.8V)	DPR (O) (0/1.8V)	25
24	GPIO_7 (I/O) (0/1.8V)	GPIO_11 (I/O) (0/1.8V)	23
22	GPIO_6 (I/O)(0/1.8V)	CONFIG_0	21
20	GPIO_5 (I/O)(0/1.8V)	CONNECTOR KEY B	
	CONNECTOR KEY B	CONNECTOR KEY B	
	CONNECTOR KEY B	CONNECTOR KEY B	
	CONNECTOR KEY B	CONNECTOR KEY B	
	CONNECTOR KEY B	GND	11
10	GPIO_9/DAS/DSS# (I/O)/LED_1# (I)(0/3.3V)	USB_D-	9
8	W_DISABLE1# (O)(0/3.3V)	USB_D+	7
6	FULL_CARD_POWER_OFF# (O)(0/1.8V or 3.3V)	GND	5
4	3.3 V	GND	3

Pin	Signal	Signal	Pin
2	3.3 V	CONFIG_3	1

5.2.2. Socket 2 Key C

5.2.2.1. Socket 2 Pinout (Mechanical Key C) On ~~Platform~~Platform

- ~~—~~Socket 2 pinout is intended to support WWAN+GNSS types of add-in solutions with BTO/CTO defined Host I/Fs.
- WWAN ~~can~~ makes use of USB 2.0, UBS 3.0, PCIe, M-PCIe, or SSIC host I/Fs. The actual implemented I/F is BTO/CTO defined between customer and vendor.
- The UIM and SIM Detect pins are used in conjunction with a SIM device in support of the WWAN solution.
- The DRP, AUDIO, COEX, and ANTCTL pins are supplemental functional pins in support of WWAN. Their functionality and pin definitions are described in section 3.2.
- The FULL_CARD_POWER_OFF# and the RESET# pins are unique and intended to be used when the WWAN solution is plugged into ~~Platform~~Platforms that provide a direct connection to V_{BAT} (and not a regulated 3.3 V) such as tablet ~~Platform~~Platforms. They are not used in Notebook ~~Platform~~Platforms and very thin ~~Platform~~Platforms that provide a regulated 3.3 V power rail. However, the FULL_CARD_POWER_OFF# signals should be tied to the 3.3 V power rail on the Notebook/very thin ~~Platform~~Platforms.
- The Vendor Defined pins are BTO/CTO defined between customer and vendor. See the Annex for example definitions.
- Pins labeled RESERVED should not be connected and reserved for future use/assignment.

Table 53 lists the pinout for Socket 2 (Mechanical Key C).

Table 53. Socket 2 Pinout Diagram (Mechanical Key C) on ~~Platform~~Platform

Pin	Signal	Signal	Pin
		GND	75
74	3.3 V	GND	73
72	3.3 V	RESET# (O) (0/1.8V)	71
70	ANTCTL3 GPIO_3 (MSB) (I)/RFFE_VIO (I) (0/1.8V)	COEX_RXD (I) (0/1.8V)	69
68	ANTCTL2 GPIO_2 (I)//RFFE_SCLK (I) (0/1.8V)	COEX_TXD (O) (0/1.8V)	67
66	ANTCTL1 GPIO_1 (I)/RFFE_SDATA (I/O) (0/1.8V)	GND	65
64	ANTCTL0 GPIO_0 (I) (1.8V)	VENDOR_PORT_C_3	63
62	RESERVED	VENDOR_PORT_C_2	61
60	VENDOR_PORT_B_5	GND	59
58	VENDOR_PORT_B_4	VENDOR_PORT_C_1	57
56	RESERVED	VENDOR_PORT_C_0	55
54	VENDOR_PORT_B_3	GND	53
52	VENDOR_PORT_B_2	M/REFCLKP	51
50	VENDOR_PORT_B_1	M/REFCLKN	49
48	VENDOR_PORT_B_0	GND	47
46	PEWAKE# (I/O) (0/1.8V))	M/PETp0; SSIC-TxP; USB3.1-Tx+	45
44	CLKREQ# (I/O) (0/1.8V)	M/PETn0; SSIC-TxN; USB3.1-Tx-	43
42	PERST# (O) (0/1.8V)	GND	41
40	SIM DETECT2 (O) (1.8V)	M/PERp0; SSIC-TxP; USB3.1-Rx+	39
38	UIM2-PWR (I)	M/PERn0; SSIC-TxN; USB3.1-Rx-	37
36	UIM2-DATA (I/O)	GND	35
34	UIM2-CLK (I)	SIM DETECT1 (O) (0/1.8V)	33
32	UIM2-RESET (I)	UIM1-PWR (I)	31
30	AUDIO1 I2S_WS (I/O) (0/1.8V)	UIM1-DATA (I/O)	29
28	AUDIO1 I2S_RX (I) (0/1.8V)	UIM1-CLK (I)	27
26	AUDIO1 I2S_TX (O) SLIMBUS_DAT (I/O) (0/1.8V)	UIM1-RESET (I)	25
24	AUDIO1 I2S_CLK (I/O) SLIMBUS_CLK (I/O) (0/1.8V)	CONNECTOR KEY C	
	CONNECTOR KEY C	CONNECTOR KEY C	
	CONNECTOR KEY C	CONNECTOR KEY C	
	CONNECTOR KEY C	CONNECTOR KEY C	
	CONNECTOR KEY C	VIO1.8V	15
14	VENDOR_PORT_A_3	FULL_CARD_POWER_OFF# (O) (1.8V)	13
12	VENDOR_PORT_A_2	DRP (O) (1.8V)	11
10	VENDOR_PORT_A_1	GND	9
8	VENDOR_PORT_A_0	USB_D-	7
6	3.3 V	USB_D+	5
4	3.3 V	GND	3
2	3.3 V	GND	1

5.3. SSD Socket; Socket 3 (Mechanical Key M)

This Socket pinouts and key are only intended for SSD devices. The Host I/Fs supported are PCIe with up to four lanes or SATA. The state of the PEDET pin (69) will indicate to the ~~Platform~~Platform which I/F of these two is connected. Table 54 lists the Socket 3 SSD pinout.

Table 54. Socket 3 SSD Pinout (Mechanical Key M) On ~~Platform~~Platform

Pin	Signal	Signal	Pin
		GND	75
74	3.3 V	GND	73
72	3.3 V	GND	71
70	3.3 V	PEDET (NC-PCIe/GND-SATA)	69
68	SUSCLK(32kHz) (O)(0/3.3V)	NC	67
	CONNECTOR Key M	CONNECTOR Key M	
	CONNECTOR Key M	CONNECTOR Key M	
	CONNECTOR Key M	CONNECTOR Key M	
	CONNECTOR Key M	CONNECTOR Key M	
58	NC	GND	57
56	NC	REFCLKp	55
54	PEWAKE# (I/O)(0/3.3V) or NC	REFCLKn	53
52	CLKREQ# (I/O)(0/3.3V) or NC	GND	51
50	PERST# (O)(0/3.3V) or NC	PETp0/SATA-A+	49
48	NC	PETn0/SATA-A-	47
46	NC	GND	45
44	ALERT# (I) (0/1.8V)	PERp0/SATA-B-	43
42	SMB_DATA (I/O) (0/1.8V)	PERn0/SATA-B+	41
40	SMB_CLK (I/O)(0/1.8V)	GND	39
38	DEVSLP (O)	PETp1	37
36	NC	PETn1	35
34	NC	GND	33
32	NC	PERp1	31
30	NC	PERn1	29
28	NC	GND	27
26	NC	PETp2	25
24	NC	PETn2	23
22	NC	GND	21
20	NC	PERp2	19
18	3.3 V	PERn2	17
16	3.3 V	GND	15
14	3.3 V	PETp3	13
12	3.3 V	PETn3	11

Pin	Signal	Signal	Pin
10	DAS/DSS# (I/O)/LED_1# (I)(0/3.3V)	GND	9
8	NC	PERp3	7
6	NC	PERn3	5
4	3.3 V	GND	3
2	3.3 V	GND	1

Although the pinouts in Table 54 allocates four additional 3.3 V power pins, it is not intended to increase the current sinking capability of the ~~Module~~Adapter. The intention is to further reduce the IR drop of the power under extreme high current cases and increase the robustness of the SSD devices. The maximum power consumption of this socket remains as identified in section 3.3, *SSD Socket 3 System Interface Signals*. This Socket will also accept SSD ~~devices~~ Add-in Cards that employ a Dual ~~Module~~ key~~ on Module scheme~~. The SMBus interface available on Socket 3 ~~may be~~is used by host as side band management interface for SSD configuration, monitoring SSD status, and other diagnostic purposes.

5.4. Soldered Down Pinouts Definitions

The soldered-down pinouts definitions are shown in the following figures:

- Figure 108,
  EF
  _
  Re
  f4
  19
  19
  44
  29
  \
  h
  \
  *
  ME
  RG
  EF
  OR
  MA
  T

Type 2226 LGA Pinout Using SDIO Based Socket 1 Pinout On ~~Platform~~Platform

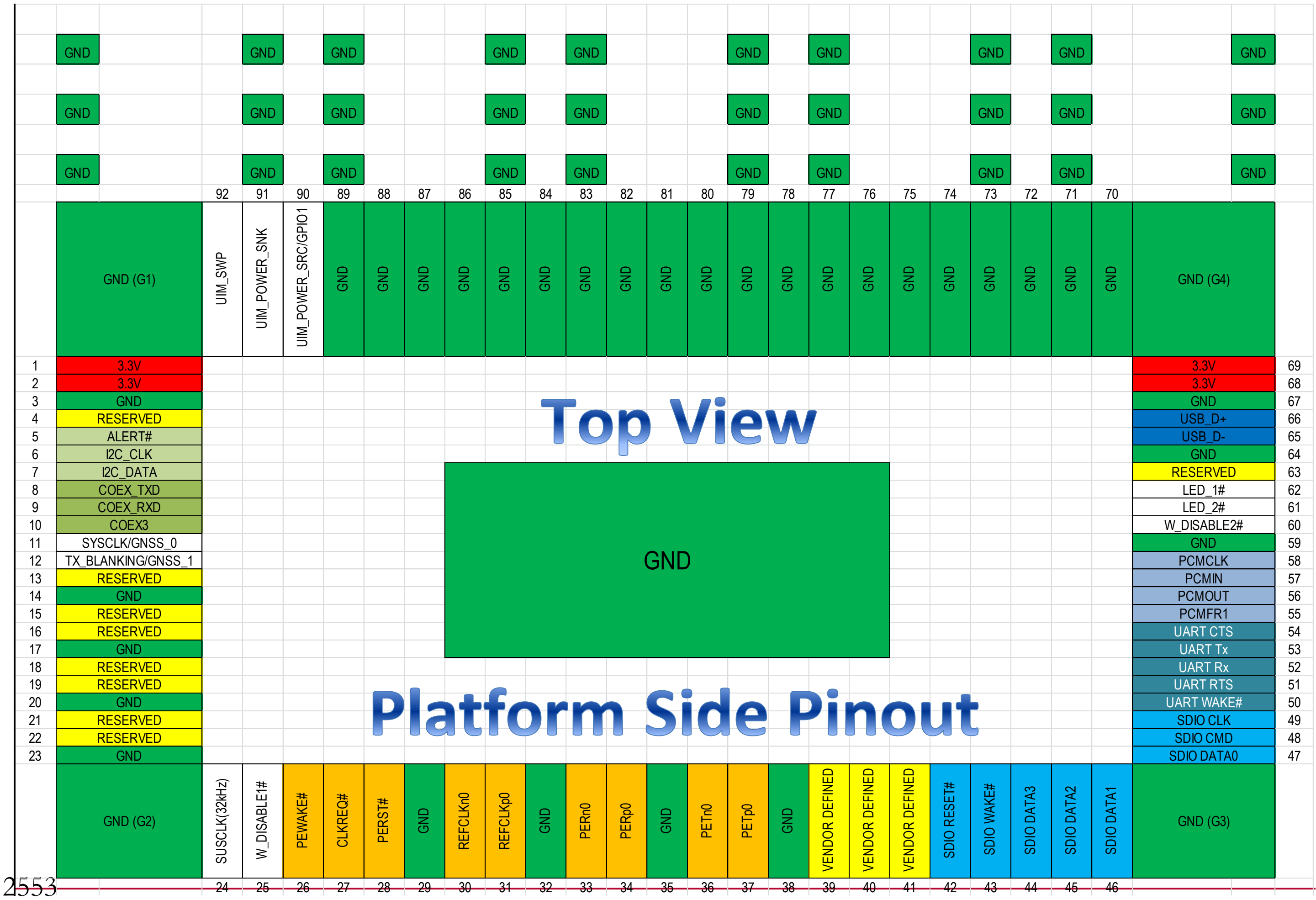
- Figure 109, EF _Ref419194447 \h * MERGEFORMAT Type 1216 LGA Pinout Using SDIO Based Socket 1 Pinout On ~~Platform~~Platform

- Figure 110, F _Ref341

101
848
\h
\
* M
ERG
EFO
RMA
T Typ
e 3026 LGA Pinout Using SDIO Based Socket 1 and Display Port Based
Socket 1 Pinout On ~~Platform~~Platform

- Figure 111,
EF
_
Re
f4
33
05
56
60
\
h
\
*
ME
RG
EF
OR
MA
T
Ty
pe 1620 BGA Pinout On Platform (Top View)

- Figure 112, EF_Ref433055698 \h * MERGEFORMAT Type 1620, Type 2024, Type 2228, Type 2828 BGA Pinout On Platform (Top View)


Top View
Platform Side Pinout
GND
GND (G1)
GND (G2)
GND (G3)
GND (G4)
92 UIM_SWP
91 UIM_POWER_SNK
90 UIM_POWER_SRC/GPIO1
89 GND
88 GND
87 GND
86 GND
85 GND
84 GND
83 GND
82 GND
81 GND
80 GND
79 GND
78 GND
77 GND
76 GND
75 GND
74 GND
73 GND
72 GND
71 GND
70 GND
1 3.3V
2 3.3V
3 GND
4 RESERVED
5 ALERT#
6 I2C_CLK
7 I2C_DATA
8 COEX_TXD
9 COEX_RXD
10 COEX3
11 SYSCLK/GNSS_0
12 TX_BLANKING/GNSS_1
13 RESERVED
14 GND
15 RESERVED
16 RESERVED
17 GND
18 RESERVED
19 RESERVED
20 GND
21 RESERVED
22 RESERVED
23 GND
24 SUSCLK(32kHz)
25 W_DISABLE1#
26 PEWAKE#
27 CLKREQ#
28 PERST#
29 GND
30 REFCLKn0
31 REFCLKp0
32 GND
33 PERn0
34 PERp0
35 GND
36 PETn0
37 PETp0
38 GND
39 VENDOR DEFINED
40 VENDOR DEFINED
41 VENDOR DEFINED
42 SDIO RESET#
43 SDIO WAKE#
44 SDIO DATA3
45 SDIO DATA2
46 SDIO DATA1
3.3V 69
3.3V 68
GND 67
USB_D+ 66
USB_D- 65
GND 64
RESERVED 63
LED_1# 62
LED_2# 61
W_DISABLE2# 60
GND 59
PCMCLK 58
PCMIN 57
PCMOUT 56
PCMFR1 55
UART CTS 54
UART Tx 53
UART Rx 52
UART RTS 51
UART WAKE# 50
SDIO CLK 49
SDIO CMD 48
SDIO DATA0 47

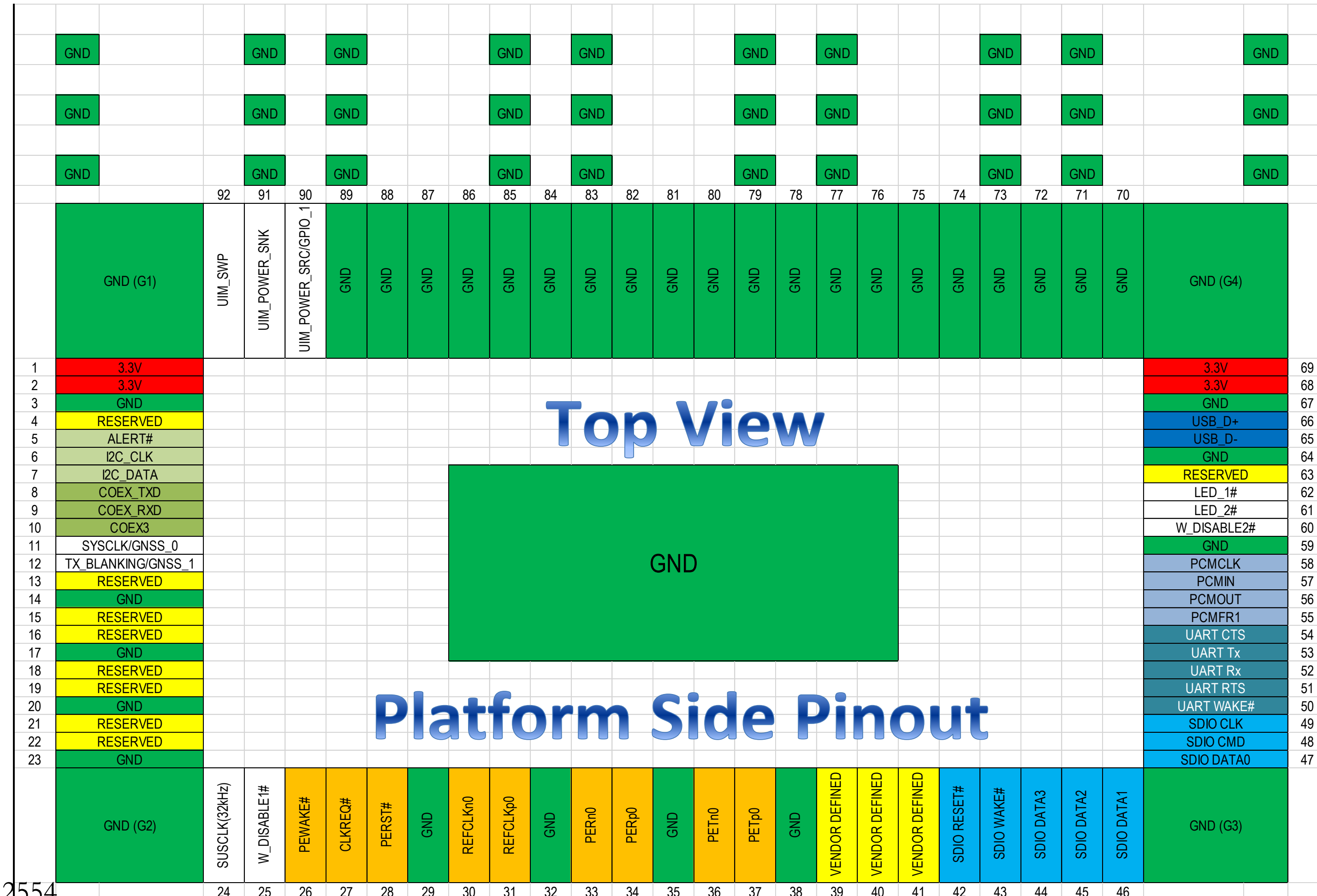
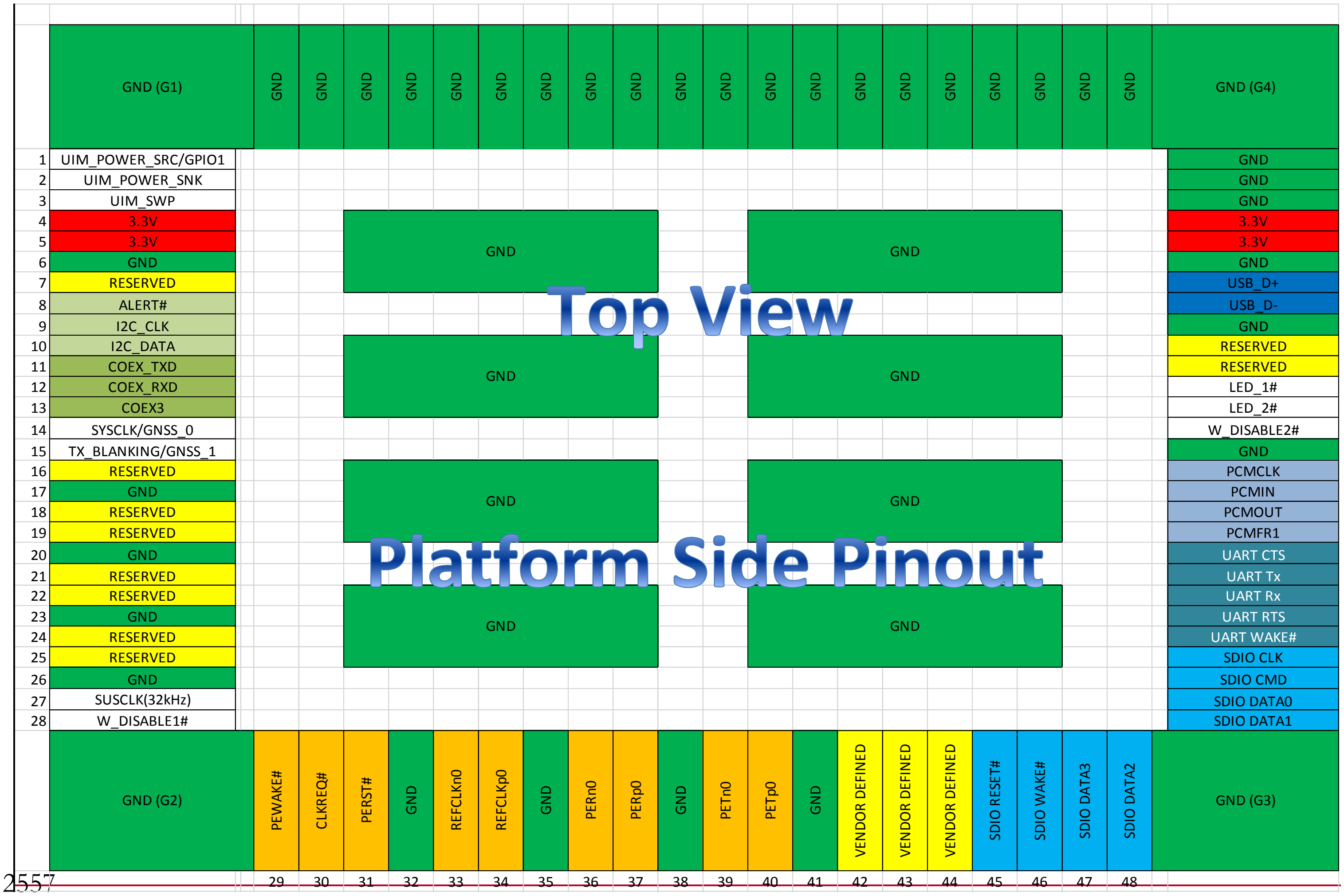


Figure 108. Type 2226 LGA Pinout Using SDIO Based Socket 1 Pinout On ~~Platform~~Platform



Top View
Platform Side Pinout
GND (G1)
GND (G4)
GND (G2)
GND (G3)
GND
1 UIM_POWER_SRC/GPIO1
2 UIM_POWER_SNK
3 UIM_SWP
4 3.3V
5 3.3V
6 GND
7 RESERVED
8 ALERT#
9 I2C_CLK
10 I2C_DATA
11 COEX_TXD
12 COEX_RXD
13 COEX3
14 SYSCLK/GNSS_0
15 TX_BLANKING/GNSS_1
16 RESERVED
17 GND
18 RESERVED
19 RESERVED
20 GND
21 RESERVED
22 RESERVED
23 GND
24 RESERVED
25 RESERVED
26 GND
27 SUSCLK(32kHz)
28 W_DISABLE1#
GND
GND
GND
3.3V
3.3V
GND
USB_D+
USB_D-
GND
RESERVED
RESERVED
LED_1#
LED_2#
W_DISABLE2#
GND
PCMCLK
PCMIN
PCMOUT
PCMFR1
UART CTS
UART Tx
UART Rx
UART RTS
UART WAKE#
SDIO CLK
SDIO CMD
SDIO DATA0
SDIO DATA1
29 PEWAKE#
30 CLKREQ#
31 PERST#
32 GND
33 REFCLKn0
34 REFCLKp0
35 GND
36 PERn0
37 PERp0
38 GND
39 PETn0
40 PETp0
41 GND
42 VENDOR DEFINED
43 VENDOR DEFINED
44 VENDOR DEFINED
45 SDIO RESET#
46 SDIO WAKE#
47 SDIO DATA3
48 SDIO DATA2

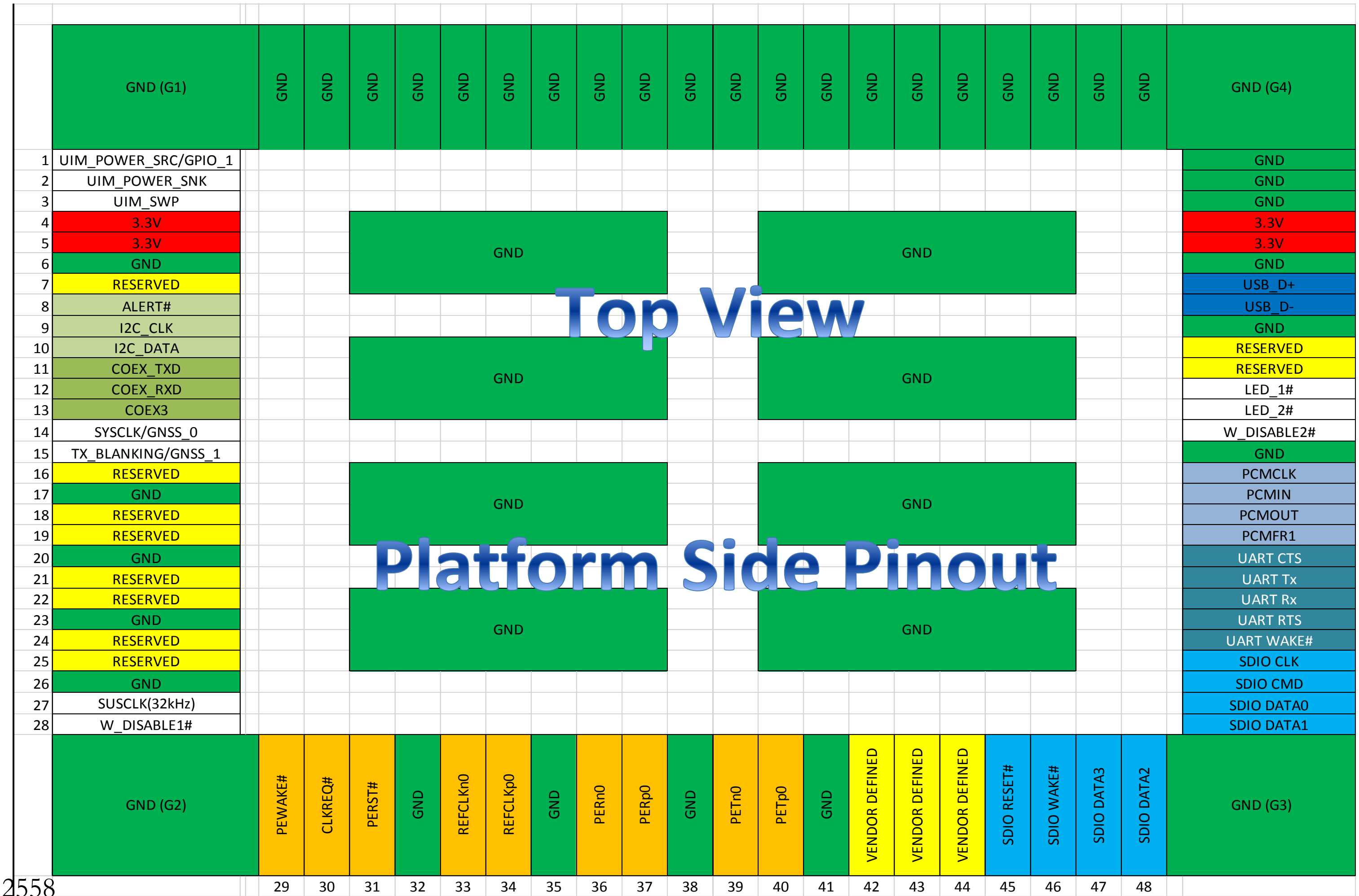
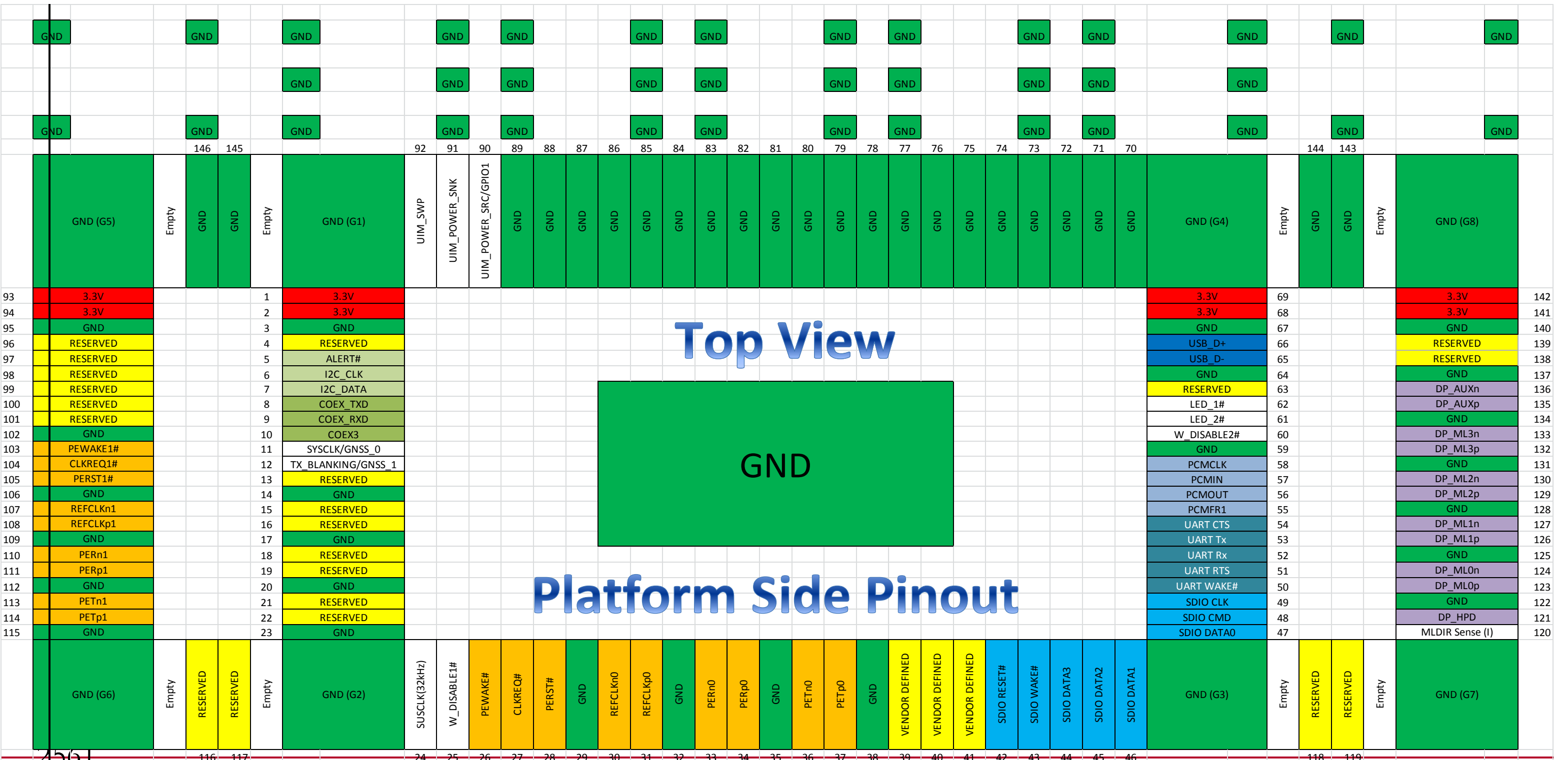


Figure 109. Type 1216 LGA Pinout Using SDIO Based Socket 1 Pinout On ~~Platform~~Platform



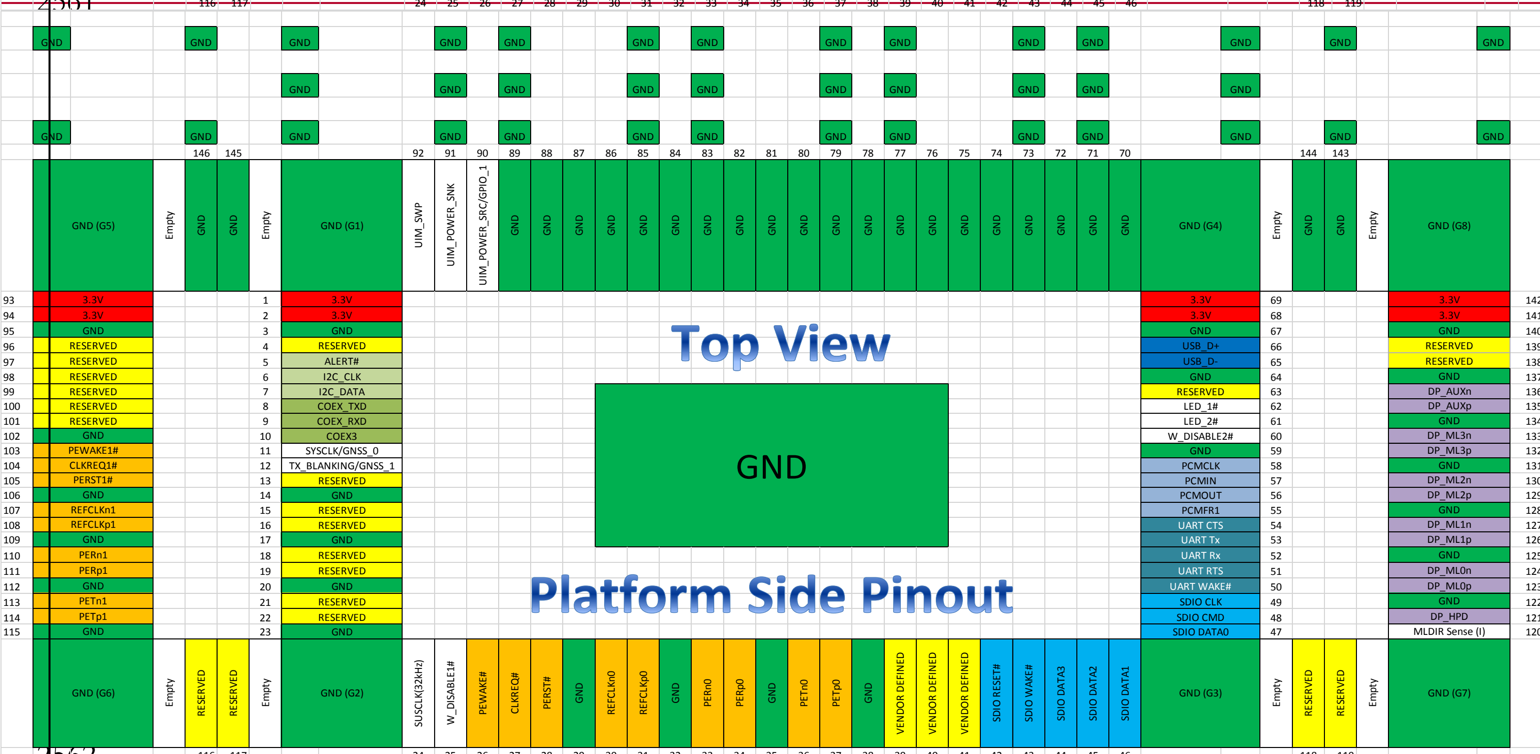


Figure 110. Type 3026 LGA Pinout Using SDIO Based Socket 1 and Display Port Based Socket 1 Pinout On ~~Platform~~Platform

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
B	DNU	DNU		DNU		CAL_P		DNU			DNU		DNU		DNU		DNU	DNU
C	GND	GND	GND	GND	GND	DNU	XTAL_OUT	XTAL_IN	DNU	RZQ_1	DNU	DNU	RFU	RFU	GND	DNU	DNU	DNU
D				REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	+3.3 V	+3.3 V	GND	DNU	DIAG1	SUSCLK	RFU			
E	GND	GND	GND	GND	GND	GND	GND	DEVSLP	+3.3 V	+3.3 V	GND	PEWAKE#	DIAG0	GND	GND	DNU	DNU	DNU
F				SATA-A+ / PETp0	SATA-A- /PETn0	GND								PEDET	RFU			
G	GND	GND	GND	GND	GND		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		GND	GND	DNU	DNU	DNU
H				SATA-B+/PERp0	SATA-B- /PERn0		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		RFU	RFU			
J	GND	GND	GND	GND	GND		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		GND	GND	DNU	DNU	DNU
K				PETp1	PETn1		GND	GND	GND	GND	GND	GND		RFU	RFU			
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JTAG_ TRST#
M				PERp1	PERn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU			
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_ TCK	JTAG_ TMS
P				PETp2	PETn2		GND	GND	GND	GND	GND	GND		RFU	RFU			
R	GND	GND	GND	GND	GND		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		GND	GND	DNU	JTAG_ TDI	JTAG_ TDO
T				PERp2	PERn2		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		RFU	RFU			
U	GND	GND	GND	GND	GND		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		GND	GND	DNU	SMB_ CLK	SMB_ DATA
V				PETp3	PETn3									RFU	RFU			
W	GND	GND	GND	GND	GND	GND	LED1#/ DAS	RFU	+3.3 V	+3.3 V	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#
Y				PERp3	PERn3	GND	DNU	DNU	+3.3 V	+3.3 V	GND	DNU	GND	DNU	DNU			
AA	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	RZQ_2	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU
AB	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
B	DNU	DNU		DNU		CAL_P		DNU			DNU		DNU		DNU		DNU	DNU
C	GND	GND	GND	GND	GND	DNU	XTAL_OUT	XTAL_IN	DNU	RZQ_1	DNU	DNU	RFU	RFU	GND	DNU	DNU	DNU
D				REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	3.3 V	3.3 V	GND	DNU	DIAG1	SUSCLK	RFU			
E	GND	GND	GND	GND	GND	GND	GND	DEVSLP	3.3 V	3.3 V	GND	PEWAKE#	DIAG0	GND	GND	DNU	DNU	DNU
F				SATA-A+ / PETp0	SATA-A- /PETn0	GND								PEDET	RFU			
G	GND	GND	GND	GND	GND		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		GND	GND	DNU	DNU	DNU
H				SATA-B+/PERp0	SATA-B- /PERn0		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		RFU	RFU			
J	GND	GND	GND	GND	GND		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		GND	GND	DNU	DNU	DNU
K				PETp1	PETn1		GND	GND	GND	GND	GND	GND		RFU	RFU			
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JTAG_ TRST#
M				PERp1	PERn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU			
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_ TCK	JTAG_ TMS
P				PETp2	PETn2		GND	GND	GND	GND	GND	GND		RFU	RFU			
R	GND	GND	GND	GND	GND		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		GND	GND	DNU	JTAG_ TDI	JTAG_ TDO
T				PERp2	PERn2		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		RFU	RFU			
U	GND	GND	GND	GND	GND		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		GND	GND	DNU	SMB_ CLK	SMB_ DATA
V				PETp3	PETn3									RFU	RFU			
W	GND	GND	GND	GND	GND	GND	LED1#/ DAS	RFU	3.3 V	3.3 V	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#
Y				PERp3	PERn3	GND	DNU	DNU	3.3 V	3.3 V	GND	DNU	GND	DNU	DNU			
AA	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	RZQ_2	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU
AB	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU

(empty box)	=>	No solder ball

Figure 111. Type 1620 BGA Pinout On ~~Platform~~Platform (Top View)

Type 2828	Type 2228	Type 2024	Type 1620	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
								1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24				
											1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18							
A				DNU	DNU																													DNU	DNU
B	A			DNU				DNU	DNU	DNU	DNU	DNU															DNU	DNU	DNU	DNU	DNU				DNU
C	B	A						DNU	DNU	DNU																			DNU	DNU	DNU				
D	C	B						DNU	DNU																					DNU	DNU				
E	D	C						DNU																							DNU				
F	E	D	A	DNU				DNU			DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU			DNU				DNU
G	F	E	B								DNU	DNU		DNU		CAL_P		DNU			DNU		DNU		DNU		DNU	DNU							
H	G	F	C	DNU					DNU		GND	GND	GND	GND	GND	DNU	XTAL_OUT	XTAL_IN	DNU	RZQ_1	DNU	DNU	RFU	RFU	GND	DNU	DNU	DNU		DNU					DNU
J	H	G	D											REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	3.3 V	3.3 V	GND	DNU	DIAG1	SUSCLK	RFU										
K	J	H	E	DNU				DNU			GND	GND	GND	GND	GND	GND	GND	DEVSLP	3.3 V	3.3 V	GND	PEWAKE#	DIAG0	GND	GND	DNU	DNU	DNU			DNU				DNU
L	K	J	F											SATA-A+ /PETp0	SATA-A- /PETn0	GND								PEDET	RFU										
M	L	K	G	DNU				DNU			GND	GND	GND	GND	GND		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		GND	GND	DNU	DNU	DNU			DNU				DNU
N	M	L	H											SATA-B+ /PERp0	SATA-B- /PERn0		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		RFU	RFU										
P	N	M	J					DNU			GND	GND	GND	GND	GND		1.2 V	1.2 V	GND	GND	1.2 V	1.2 V		GND	GND	DNU	DNU	DNU			DNU				
R	P	N	K											PETp1	PETn1		GND	GND	GND	GND	GND	GND		RFU	RFU										
T	R	P	L					DNU			GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JTAG_TRST#			DNU				
U	T	R	M											PERp1	PERn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU										
V	U	T	N					DNU			GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_TCK	JTAG_TMS			DNU				
W	V	U	P											PETp2	PETn2		GND	GND	GND	GND	GND	GND		RFU	RFU										
Y	W	V	R					DNU			GND	GND	GND	GND	GND		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		GND	GND	DNU	JTAG_TDI	JTAG_TDO			DNU				
AA	Y	W	T											PERp2	PERn2		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		RFU	RFU										
AB	AA	Y	U	DNU				DNU			GND	GND	GND	GND	GND		1.8 V	1.8 V	GND	GND	1.8 V	1.8 V		GND	GND	DNU	SMB_CLK	SMB_DATA			DNU				DNU
AC	AB	AA	V											PETp3	PETn3									RFU	RFU										
AD	AC	AB	W	DNU				DNU			GND	GND	GND	GND	GND	GND	LED1#/ DAS	RFU	3.3 V	3.3 V	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#			DNU				DNU
AE	AD	AC	Y											PERp3	PERn3	GND	DNU	DNU	3.3 V	3.3 V	GND	DNU	GND	DNU	DNU										
AF	AE	AD	AA	DNU					DNU		GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	RZQ_2	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU		DNU					DNU
AG	AF	AE	AB								DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU							
AH	AG	AF	AC	DNU				DNU			DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU			DNU				DNU
AJ	AH	AG						DNU																							DNU				
AK	AJ	AH						DNU	DNU																					DNU	DNU				
AL	AK	AJ						DNU	DNU	DNU																			DNU	DNU	DNU				
AM	AL			DNU				DNU	DNU	DNU	DNU	DNU															DNU	DNU	DNU	DNU	DNU				DNU
AN				DNU	DNU																													DNU	DNU

	Type 1620
	Type 2024
	Type 2228
	Type 2828

Figure 112. Type 1620, Type 2024, Type 2228, Type 2828 BGA Pinout On ~~Platform~~Platform (Top View)

2574 6

2575
6. Annex

2576
6.1. Glossary

A	Amperage or Amp	**NIC**	Network Interface Card
BGA	Ball Grid Array	**NC**	Not Connected
BIOS	Basic Input Output System	**OD**	Open Drain
BTO	Build-to-Order	**OEM**	Original Equipment Manufacturer
CEM	Card Electromechanical	**OS**	Operating System
CTO	Configure To Order	**PCIe**	Peripheral Component Interconnect Express
DC	Direct Current	**SATA**	Serial Advanced Technology Attachment or Serial ATA
DNU	Do Not Use	**PCM**	Pulse Code Modulation
DPR	Dynamic Power Reduction	**RF**	Radio Frequency
GND	Ground	**RFU**	Reserved for Future Use
GNSS	Global Navigation Satellite System (GPS+GLONASS)	**RMS**	Root Mean Square
HDR	Hybrid Digital Radio	**RoHS**	Restriction of Hazardous Substances Directive
HSIC	High Speed Inter-Chip	**RSS**	Root Sum Square
I/F	Interface	**RTC**	Real Time Clock
I/O (O/I)	Input/Output (Output/Input)	**SDIO**	Secure Digital Input Output
IR	Current x Resistance = Voltage	**SIM**	Subscriber Identity Module
I^{2}C	Inter-Integrated Circuit	**SSD**	Sold-State Drive
I2S	Integrated Interchip Sound	**SSIC**	Super Speed USB Inter-Chip
LED	Light Emitting Diode	**RF**	Radio Frequency
LGA	Land Grid Array	**USB**	Universal Serial Bus
M-PCIe	Mobile PCIe	**UART**	Universal Asynchronous Receive Transmit
mΩ	milli Ohm	**V**	Voltage
mA	milli Amp	**W**	Wattage or Watts
mV	milli Volt	**WiGig**	60 GHz multi-gigabit speed wireless communication
NFC	Near Field Communications	**WLAN**	Wireless Local Area Network
M.2	Formally called Next Generation Form Factor (NGFF)	**WPAN**	Wireless Personal Area Network
NB	Notebook	**WWAN**	Wireless Wide Area Network

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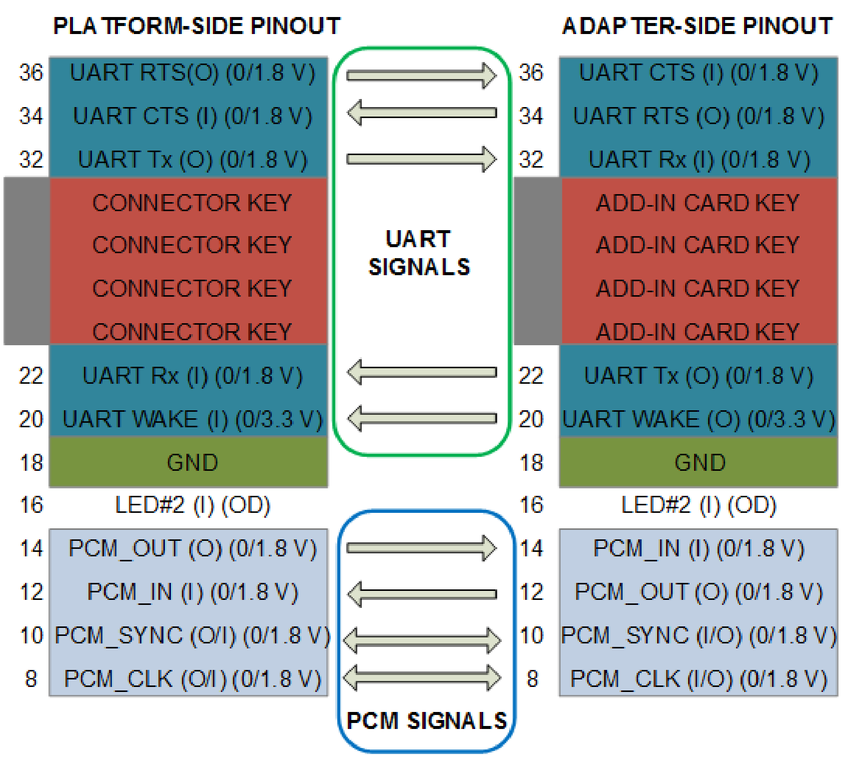
6.2. M.2 Signal Directions

This section describes the directionality of some of the interface signals incorporated in the various pinouts. Because some signals have directionality associated with them, their names and locations may be different between the ~~Platform~~Platform side and the ~~Module~~ Adapter side.

The Adapter ~~Module~~ pinouts are described in Chapter 3~~3~~ and ~~Platform~~Platform pinouts are described in Chapter 5~~5~~.

The main differences between ~~Platform~~Platform-side pinouts and ~~Module~~Add-in Card-side pinouts are shown in
Figure 113 and Figure 114.



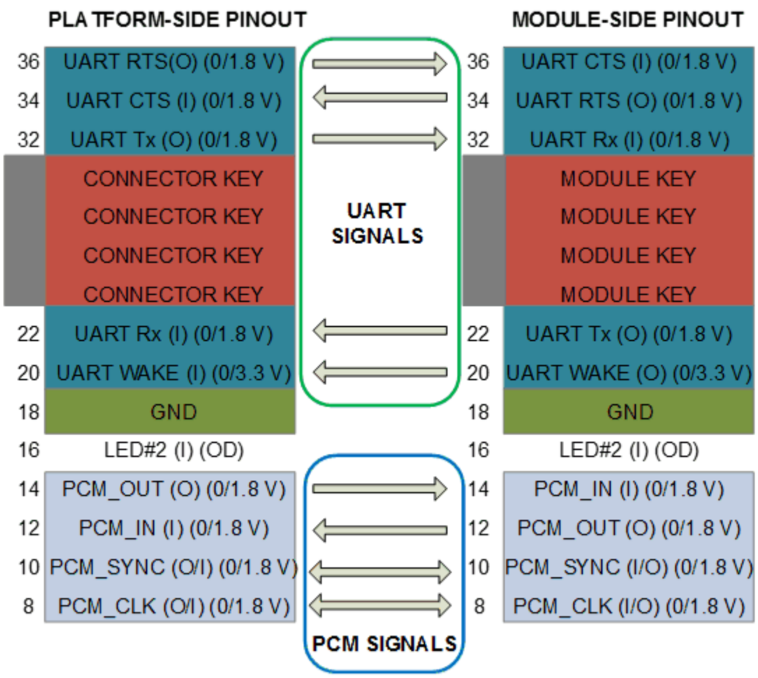
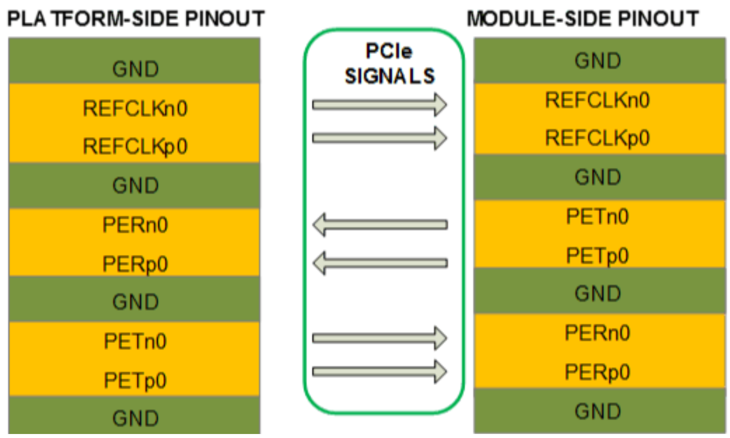


Figure 113. UART and PCM Signal Direction and Signal Name Changes



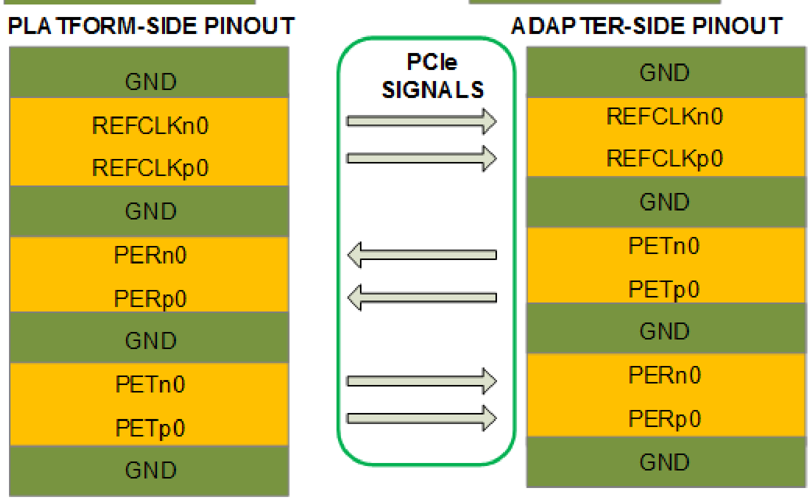
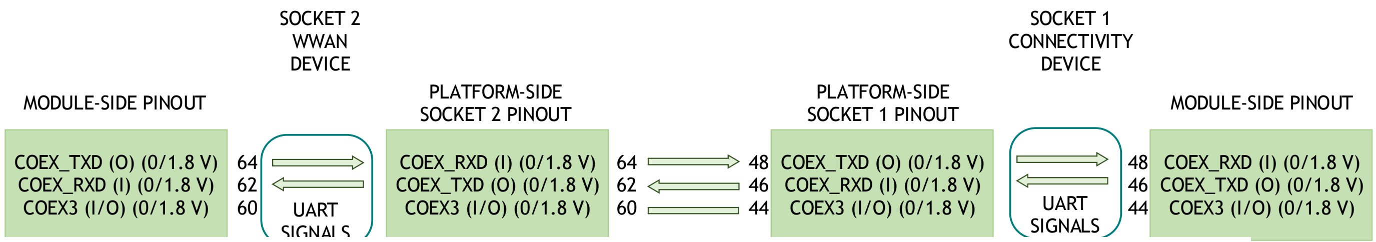


Figure 114. PCIe Signal Direction and Signal Name Changes

PCIe Pin order shown in Figure 114 coincides with Socket 1 pinouts. Alternate PCIe pin order exists in Socket 2 and 3.

Figure 113 and Figure 114 are examples of signaling directions and name changes from ~~Platform~~Platform to ~~module~~Adapter. Other cases exist for other signals in various Sockets, such as the USB3.1 Tx and Rx, SSIC_Tx and SSIC_Rx.

The two COEX signals between the WWAN device on Socket 2 and the Connectivity device on Socket 1 have defined directions. At the ~~platform~~Platform, the three COEX signals should be connected pin-to-pin as shown in Figure 115.



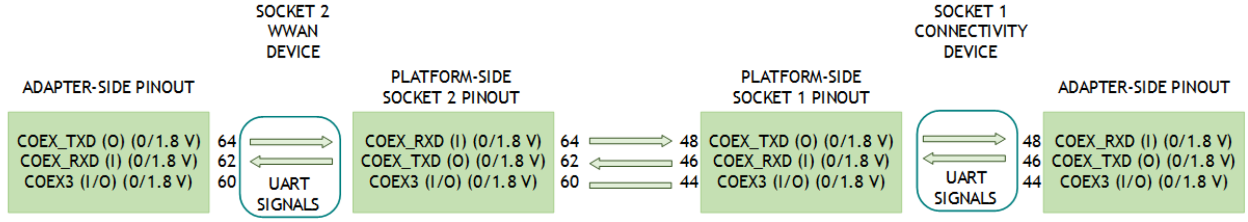


Figure 115. COEX_TXD and COEX_RXD Signal Direction

6.3. Signal Integrity Guideline

Table 55 follows the 8.0 GT/s of *PCI Express Card Electromechanical Specification* because it is the highest data rate of M.2's current application. The measurement includes connector solder pads of main board and gold finger pads of ~~module~~the Add-in Card.

It is recommended to use an electrical test fixture for evaluating connector signal integrity~~An electrical test fixture must be used for evaluating connector signal integrity~~. ~~Section 6.3.1 is provided with test fixture requirements and recommendations.~~

Table 55. Signal Integrity ~~Requirements~~ Parameters and Test Procedures for M.2 Connectors

Parameter	Procedure	~~Requirements~~Recommendations
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: • The measured differential S-parameter shall be referenced to 85 Ω differential impedance. • The test fixture shall meet the test fixture ~~requirement~~ recommendations defined in Section 6.3.1. • The test fixture effect shall be removed from the measured S-parameters. See Note 1.	≥ -0.5 dB up to 2.5 GHz; ≥ -[0.8*(f-2.5) + 0.5] dB for 2.5 GHz < f ≤ 5 GHz (e.g.~~for example~~, ≥ -2.5 dB at f = 5 GHz); ≥ -[3.0*(f-5) + 2.5] dB for 5 GHz < f ≤ 12 GHz (~~for example~~e.g., ≥ -10 dB at f = 7.5 GHz)
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: • The measured differential S-parameter shall be referenced to 85 Ω differential impedance. • The test fixture shall meet the test fixture recommendations ~~requirement~~ defined in Section 6.3.1. • The test fixture effect shall be removed from the measured S-parameters. See Note 1.	≤ -15 dB up to 3 GHz; ≤ 5*f - 30 dB for 3 GHz < f ≤ 5 GHz; ≤ -1 dB for 5 GHz < f ≤ 12 GHz
Intra-pair Skew (Soldered-down BGA)	Intra-pair skew must be achieved by design; measurement not required.	1 ps max
Intra-pair Skew (BGA mounted on the M.2 ~~module~~Add-in Card)	Intra-pair skew must be achieved by design; measurement not required.	2 ps max

Parameter	Procedure	~~Requirements~~Recommendations
Differential Near End Crosstalk (DDNEXT) and Differential Far End Crosstalk (DDFEXT)	EIA 364-90 The EIA standard must be used with the following considerations: • The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector. • This is a differential crosstalk between a victim differential signal pair and all adjacent differential signal pairs. The measured differential S--parameter shall be referenced to 85 Ω differential impedance.	≤ -32 dB up to 2.5 GHz; ≤ -26 dB for 2.5 GHz < f ≤ 5 GHz; ≤ -20 dB for 5 GHz < f ≤ 10 GHz < -10 dB for 10 GHz < f ≤ 12 GHz
Note 1: The specified S-parameters recommendations ~~requirements~~ are for connector only, not including the test fixture effect. While the TRL calibration method is recommended, other calibration methods are allowed.		

6.3.1. Test Fixture Recommendations~~Requirements~~

The test fixture for connector S-parameter measurement shall be designed and built to the following recommendations~~requirements~~:

- The test fixture shall be an FR4-based PCB of the microstrip structure where the dielectric thickness of this structure shall be approximately 0.102 mm (4 mils).
- The total thickness of the test fixture PCB shall be 0.8 mm (31.5 mils) and the test ~~add~~Add-in ~~module c~~Card should be a break-out card fabricated in the same PCB panel for the fixture.
- The trace lengths between the connector and measurement port shall be minimized. The maximum trace length shall not exceed 45.72 mm (1,800 mils). The trace lengths between the connector and measurement port on the test ~~main~~ baseboard and ~~module~~ test Add-in Card shall be equal. Note that the gold finger pad is not counted as the trace of the ~~module~~Add-in Card; it is considered as a part of the connector interface.
- All of the traces on the test main board and test A~~a~~dd-in ~~module c~~Card must be held to a characteristic impedance of 50 Ω with a tolerance of ±7%, and they should be uncoupled.
- Use of SMA connectors as measurement ports is recommended. The SMA launch structure shall be designed to minimize the connection discontinuity from SMA to the trace. The impedance range of the SMA seen from a TDR with a 30 ps rise time is recommended to be within 50 Ω ±7 Ω

Figure 116, Figure 117, and Figure 118 show the recommended pad and anti-pad guideline for Signal Integrity modeling.

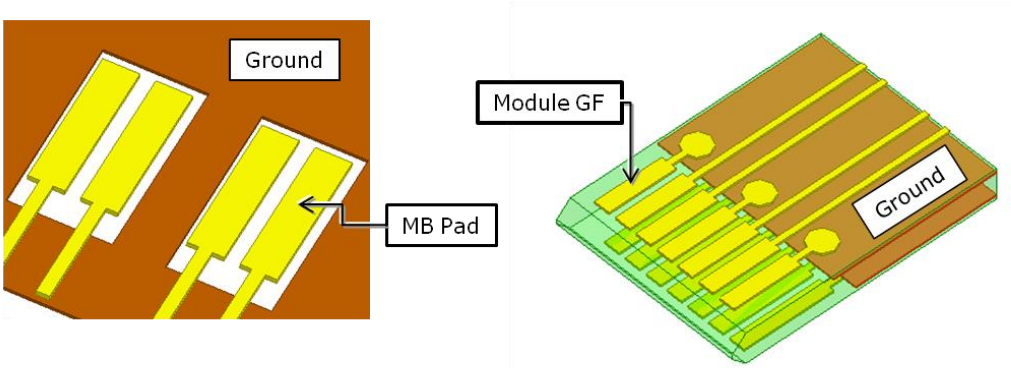


Figure 116. Suggested ~~Motherboard~~Motherboard and ~~Module Board~~Add-in Card Signals and Ground Pad Layout Guideline

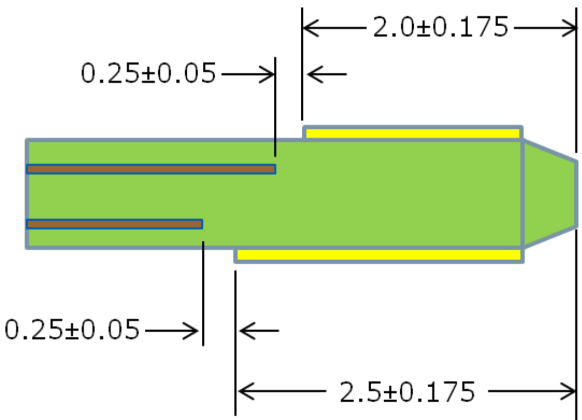


Figure 117. Suggested Ground Void for ~~Module~~ Add-in Card Simulation

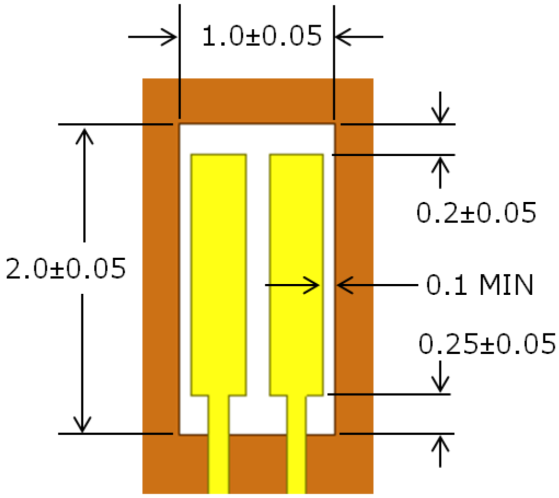


Figure 118. Suggest Ground Void for Main Board

6.3.2. Suggested Top Mount Signal Integrity PCB Layout

Suggested PCB layouts for the ~~Module~~ test Add-in Card and ~~Motherboard~~test baseboard side used to test the M.2 Top Mount Connector are given in Figure 119 and Figure 120.

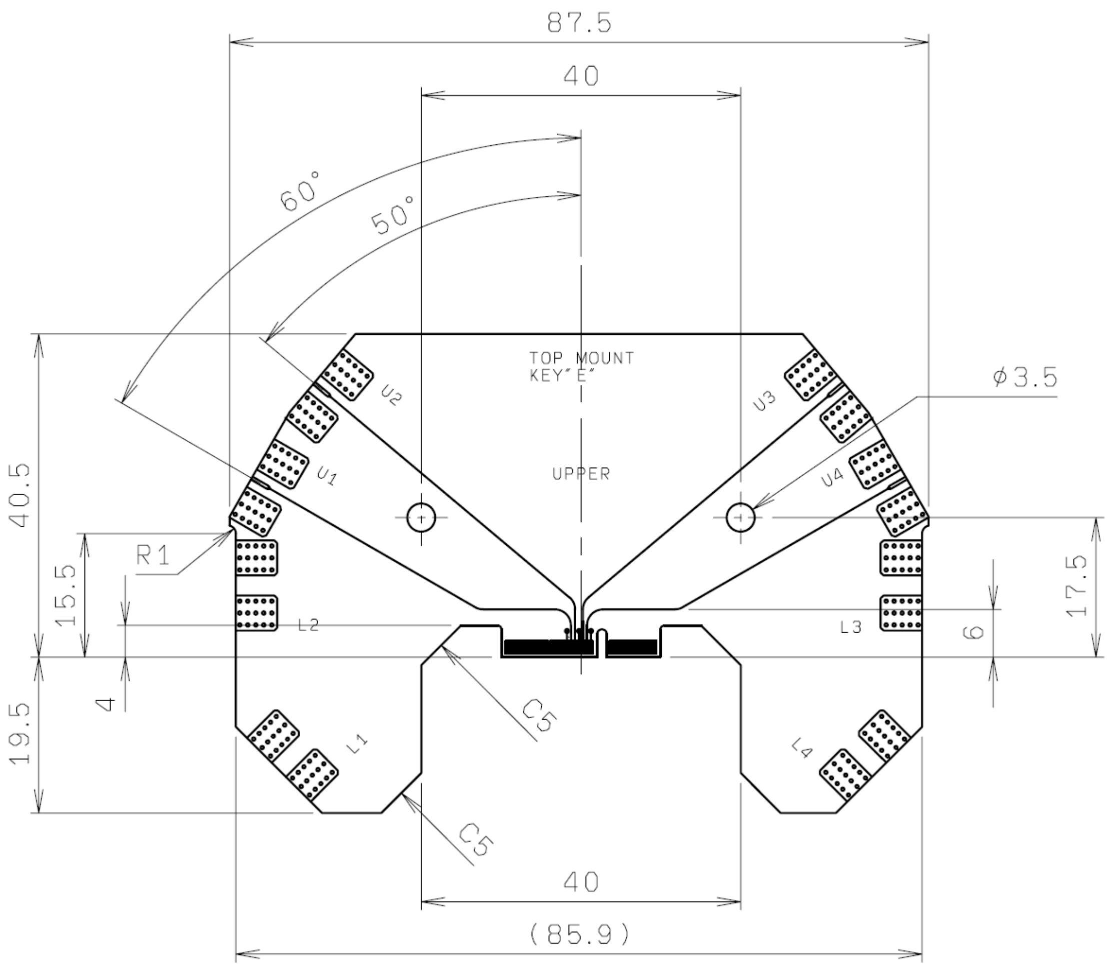


Figure 119. Top Mount ~~Module~~ Add-in Card Test Fixture PCB Layout

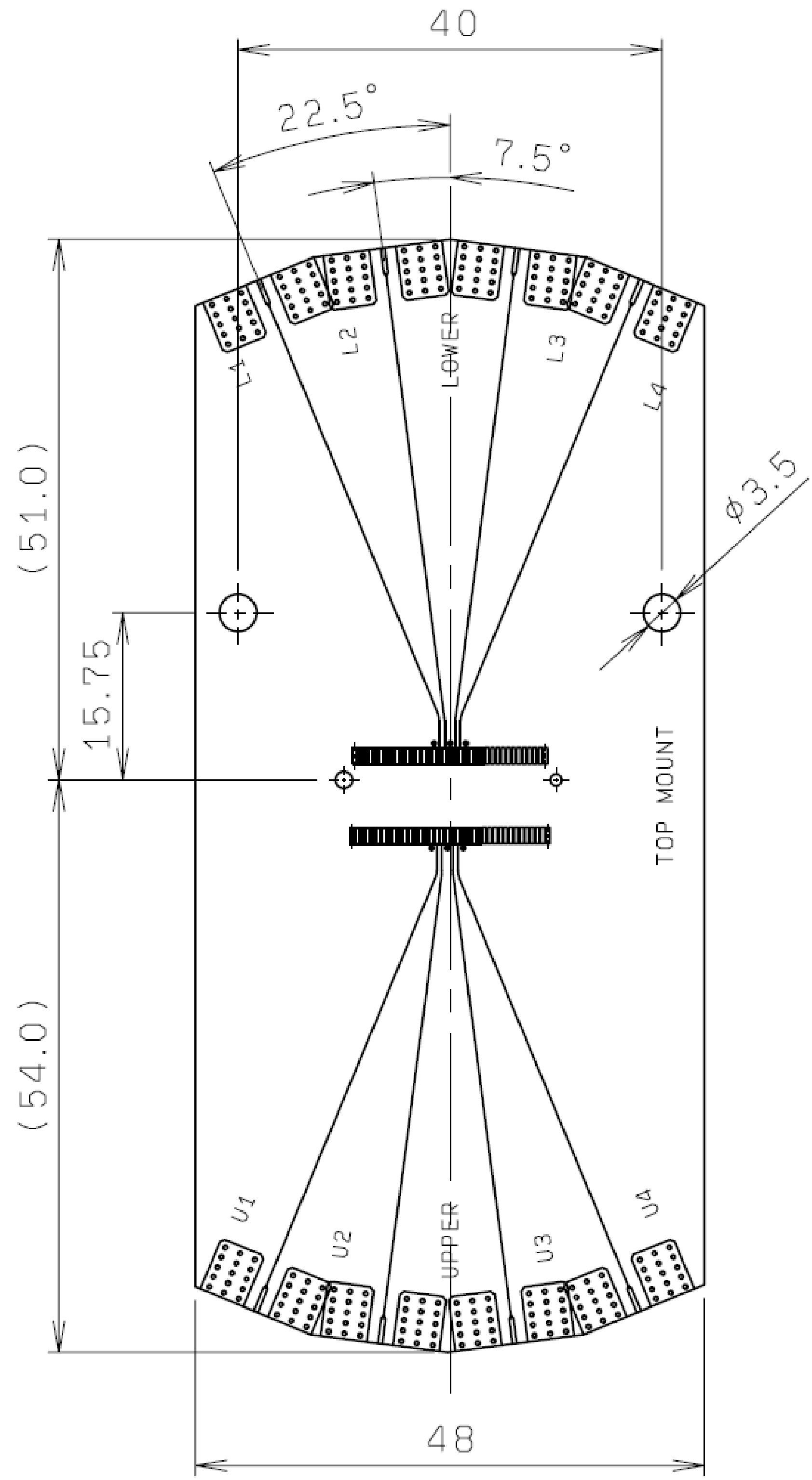


Figure 120. Top Mount ~~Mother Board~~Motherboard Test Fixture PCB

6.3.3. Suggested Mid-mount Signal Integrity PCB Layout

Suggested PCB layouts for the ~~Module~~ test Add-in Card and ~~Motherboard~~test baseboard side used to test the M.2 Mid-mount Connector are shown in the following figure:

- Figure 121. Top Mount Connector Test Fixture
- Figure 122. Mid-mount Connector Test Fixture
- Figure 123. Mid-mount Add-in Card Test Fixture PCB Layout
- Figure 124. Mid-mount Motherboard Test Fixture PCB
- Figure 125. Detail of Top-side SMA End Launch Connector Pad
- Figure 126. Ground Void on Backside
- Figure 127. Detail of Mid-mount Vias on Top-side
- Figure 128. Detail of Ground Void on Mid-mount Bottom Side .

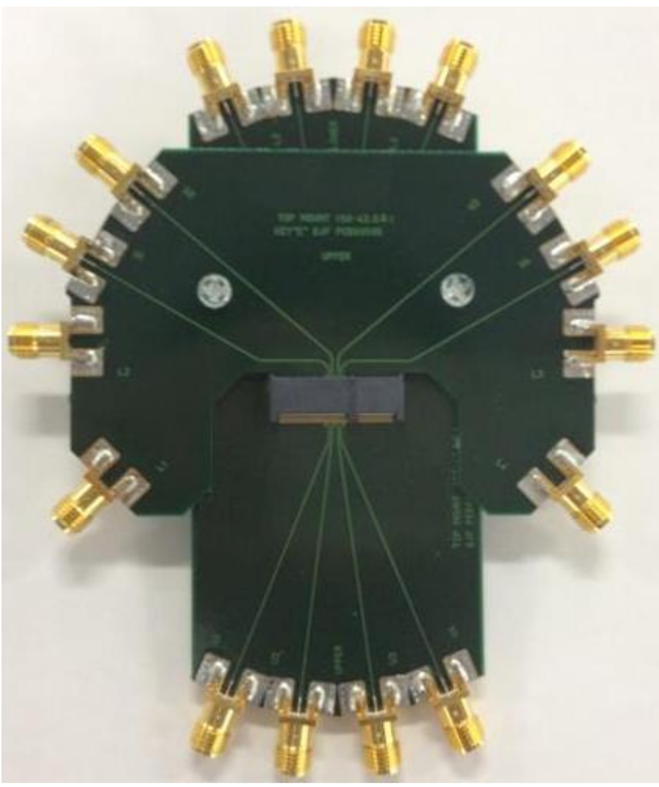


Figure 121. Top Mount Connector Test Fixture

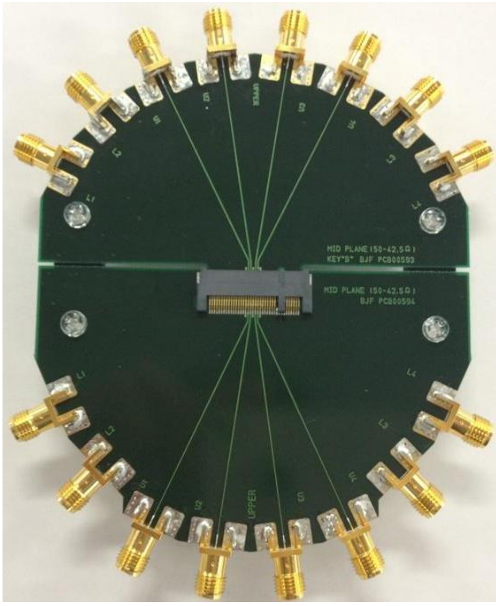


Figure 122. Mid-mount Connector Test Fixture

PCB stack-up and Trace Impedance should be designed for 85 Ω MSL

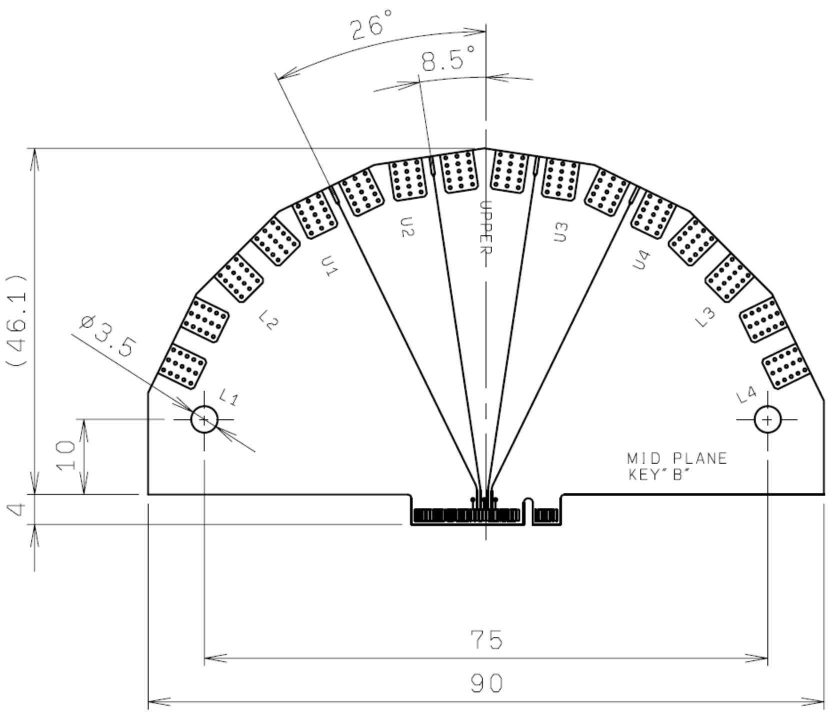


Figure 123. Mid-mount ~~Module~~ Add-in Card Test Fixture PCB Layout

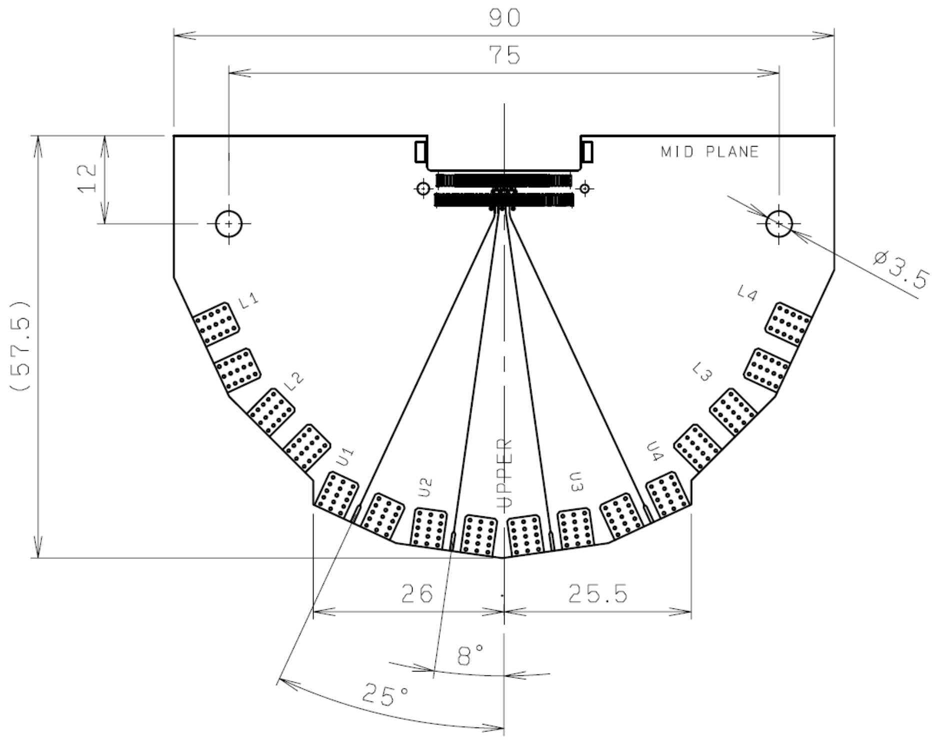


Figure 124. Mid-mount ~~Mother Board~~Motherboard Test Fixture PCB

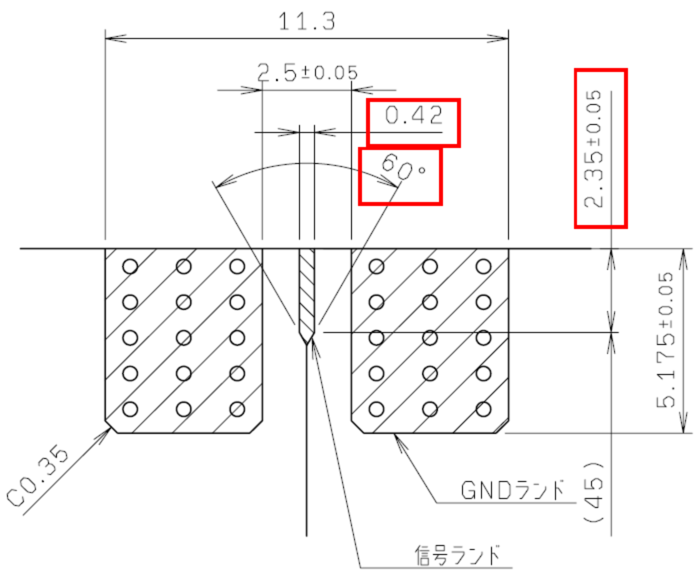


Figure 125. Detail of Top-side SMA End Launch Connector Pad

SMA pad designed for 42.5 Ω

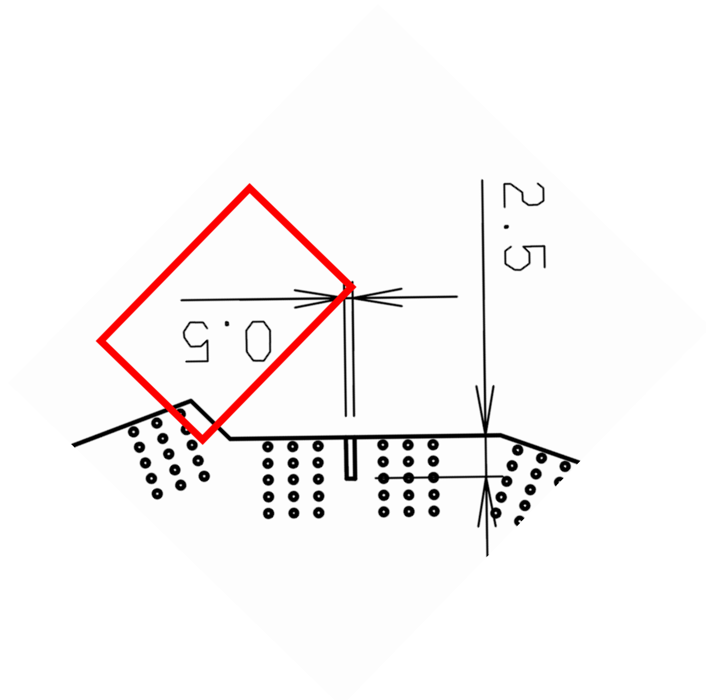


Figure 126. Ground Void on Backside

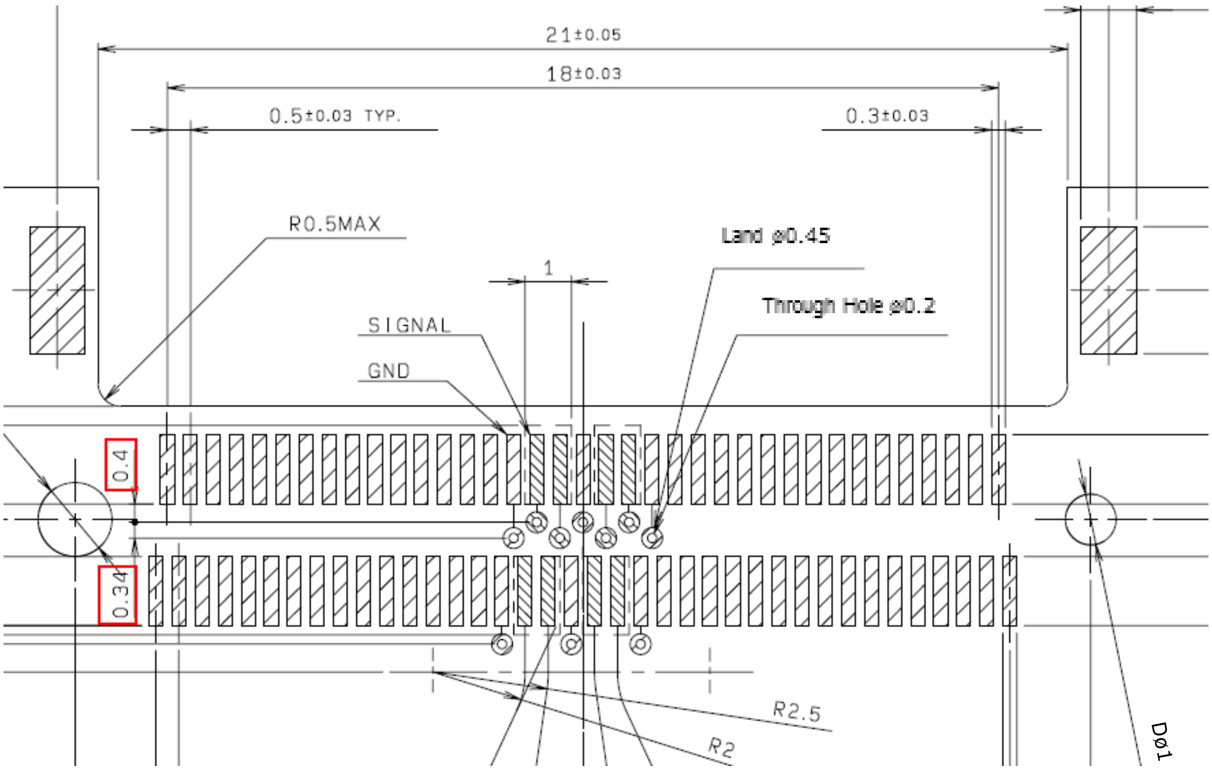


Figure 127. Detail of Mid-mount Vias on Top-side ~~Mother Board~~Motherboard

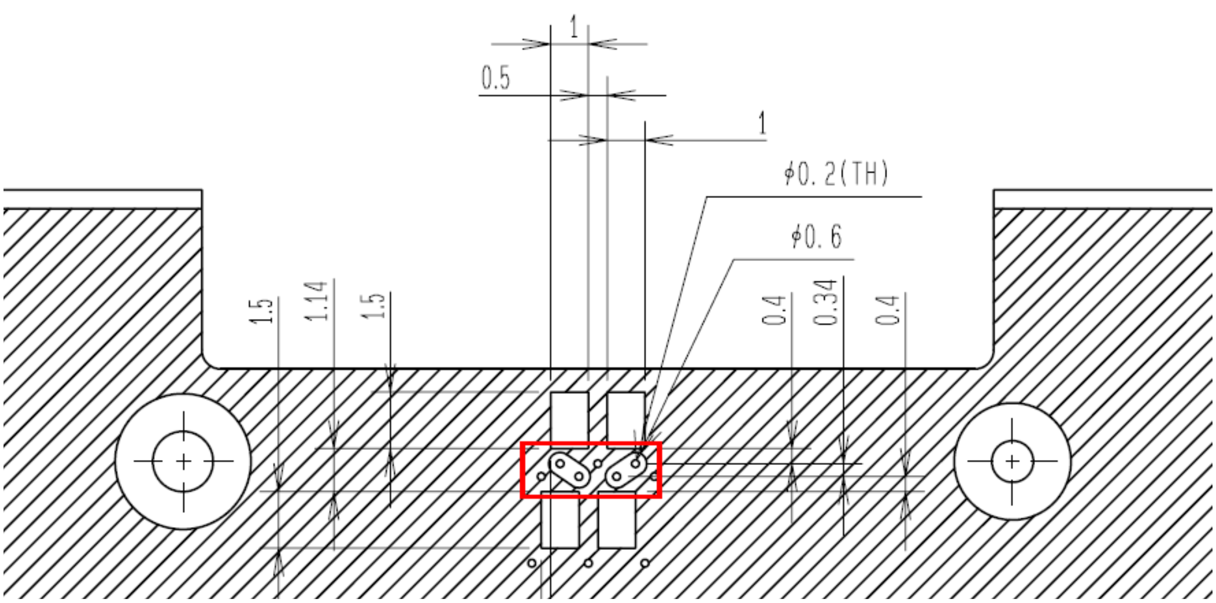


Figure 128. Detail of Ground Void on Mid-mount Bottom Side ~~Mother Board~~Motherboard

6.4. RF Connector Related Test Setups

6.4.1. VSWR Test Set-up Method for RF Connector Receptacles

Measure the VSWR of the receptacle as shown in Figure 129 with the aid of a Network Analyzer. Measure between 100 MHz and 6 GHz or alternatively for the optional enhanced connector from 100 MHz and 12 GHz.

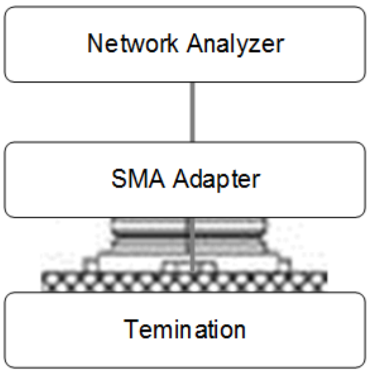


Figure 129. VSWR Test Setup for Receptacle RF Connector

6.4.2. Contact Resistance Measurement Setup ~~&~~and Test Procedure Example

Contact resistance measurement definitions are given in Figure 130.

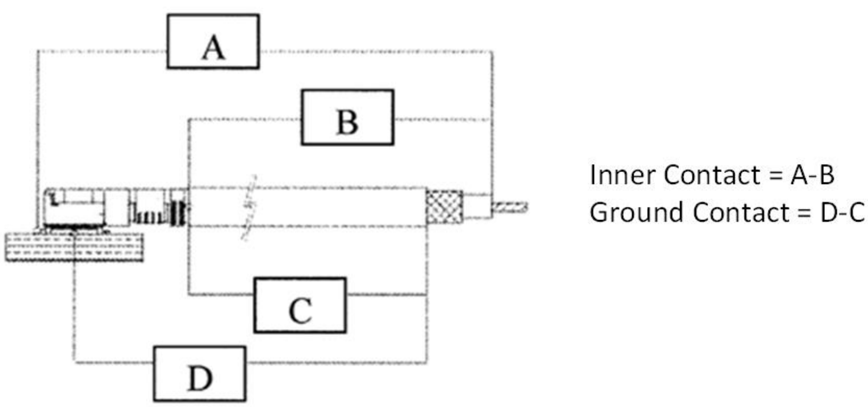


Figure 130. Contact Resistance Measurement Definitions

Step 1: Measure ten 50-mm length wire samples (prepared for plugs but un-terminated, Figure 131).

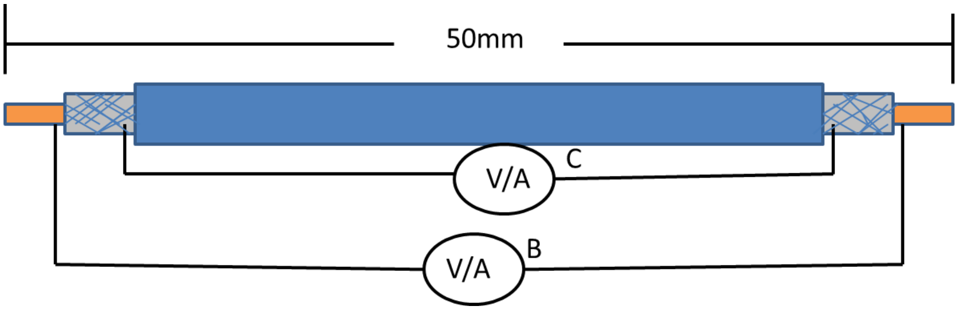


Figure 131. Prepared Wires

Example results: n=10, Unit: m-Ω

	Main (B)	GND (C)
Conductor Resistance (~~AVA~~Average)	59.020	10.920

There are variations in Center Conductor Preparation and Braid Conductor Materials. Therefore, the average of 10 wires at a length 50 mm are used for the Contact Resistance Measurements. Another variation is that this exact wire is not used when measuring the terminated mated set Cable Connector to Receptacle in the next step.

Step 2: Measurement with Plug (Figure 132).

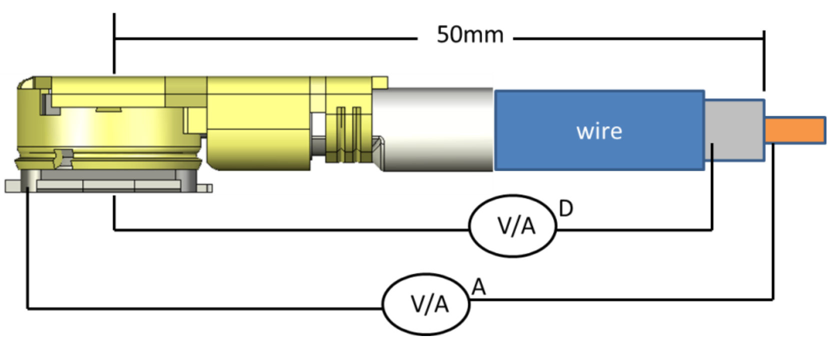


Figure 132. Prepared Wire with Plug

A = Total Measurement of the Cable Center conductor + the Connector Set Contact Resistance
D = Total Measurement of the Ground Braid conductor + the Connector Set Gnd. Resistance

Examples of measured results of the wire with plug are given in Table 56:

Table 56. Example of Prepared Wire with Plug~~, Unit: mΩ~~

	Main (A)	GND (~~C~~D)	Units
Sample 1	67.36	21.64	mΩ
Sample 2	67.61	18.61	mΩ
Sample 3	68.41	20.22	mΩ
Sample 4	68.82	19.54	mΩ
Sample 5	73.50	19.65	mΩ
Sample 6	66.41	18.76	mΩ
Sample 7	70.07	24.77	mΩ
Sample 8	68.60	19.67	mΩ
Sample 9	68.29	19.98	mΩ
Sample 10	69.37	17.52	mΩ
Average	68.845	20.036	mΩ
Maximum	73.50	24.77	mΩ
Minimum	66.41	17.52	mΩ
s (Standard Deviation)~~s~~	1.934	1.987	mΩ
+3s	74.647	25.996	mΩ

Note: Not the exact same wire is used to determine the average resistance of the wire. Variations in materials cause the resistance measurements to have various values.
Slight differences in plating may cause the resistance measurements to have various values.

Step 3: Calculate the Contact Resistance

Subtract the measured results, A-B and D-C to find the Contact Resistance for the sample wires/plugs. Example results are given in Table 57.

Table 57. Contact Resistance for the Sample Wires/Plugs~~, Unit: mΩ~~

	Main	GND (C)	Units
Sample 1	8.34	10.72	mΩ
Sample 2	8.59	7.69	mΩ
Sample 3	9.39	9.30	mΩ
Sample 4	9.80	8.62	mΩ
Sample 5	14.48	8.73	mΩ
Sample 6	7.39	7.84	mΩ
Sample 7	11.05	13.85	mΩ
Sample 8	9.58	8.75	mΩ
Sample 9	9.27	9.06	mΩ
Sample 10	10.35	6.60	mΩ
Average	9.825	9.116	mΩ
Maximum	14.48	13.85	mΩ
Minimum	7.39	6.60	mΩ
s (Standard Deviation)	1.934	1.987	mΩ
+3s	15.627	15.076	mΩ
Spec	20.0 Max		
Judge	OK	OK	

Based on the sample results, the Initial Contact Resistance is defined as 20 mΩ to make sure wire/plug variations are covered.

6.5. Thermal Guideline Annex

This section details examples of ~~module~~ Adapter and system skin (casing) thermal response to thermal and dissipation boundary conditions in systems. The boundary conditions vary by system, as do the skin temperature limits.

6.5.1. Assumptions

6.5.1.1. Die Thermal Dissipation Overview

Assumptions for typical components and dissipation for several Adapter ~~module~~ types are given in Table 58~~Table 55~~. Keep in mind the definition of ~~thermal design power (~~TDP~~)~~ given ~~above~~in Section 2.6.2.1. Note that the maxima given here do not necessarily correspond to their actual use in a system; these values are, from the die perspective, what they would dissipate when running all the time at their maximum capacity. The system use case scenarios make assumptions about how much of the time the devices would run and scale the dissipation accordingly. The TDP ~~thermal design power~~ therefore is different from the thermal dissipation given in Table 58.

Table 58. Assumptions for Typical Components and Dissipation

Adapter ~~Module~~ Type	**Die #**	**Function**	**Thermal Dissipation Estimates**	**Adapter ~~Module~~ Total Dissipation (Not Necessarily TDP)**	**Power Allocation**	**Power Map**
WiFi/BT	1	WiFi/BT	2	2	100%	WiFi/BT
WWAN	1	Baseband	1.2	1.9 Typical 3.25 Worst	32%	Uniform
	2	Power Mgmt			14%	
	3	RF Transceiver	0.4		11%	
	4	PA	0.3 Typ / 1.65 Worst		43%	
SSD	1	ASIC	1.5	1.74	86%	Uniform
	2	DRAM	0.05		3%	
	3	NAND1	0.03 Typ / 0.25 Worst		2%	
	4	NAND2	0.03 Typ / 0.25 Worst		2%	
	5	NAND3	0.03 Typ / 0.25 Worst		2%	
	6	NAND4	0.03 Typ / 0.25 Worst		2%	
	7	POWER	0.07		4%	
WiGig	1	WiFi/BT	2	3	67%	WiFi/BT
	2	WiGig	1		33%	WiFi no BT

Note: For comparison, maximum dissipations for WWAN components vary by technology, and are shown in Table 59. Most of these are in the 3 W range.

~~For comparison, maximum dissipations for WWAN components can vary by technology, and are shown in Table 59. Most of these are in the 3 W range.~~

Table 59. Maximum Dissipation for WWAN Adapters ~~Modules~~

WWAN Technology	Maximum Dissipation, W (not necessarily ~~Thermal Design Power~~TDP)
W-CDMA HSDPA 1900 @ 22 dBm	3.0 ± 0.1
W-CDMA HSDPA 850 @ 22 dBm	2.9 ± 0.1
W-CDMA HSDPA 2100 @ 22 dBm	2.7
CDMA 1xEVDO @ 24 dBm	2.8 ± 0.1
GPRS Class 10 @ 32 dBm	1.8
LTE @ 22 dBm	3.1 ± 0.1

6.5.1.2. Component Overview

Generic assumptions for package designations and types expected to populate Adapters ~~modules~~ are listed in Table 60.

Table 60. Generic Assumptions for Package Designations and Types Expected to Populate Adapters ~~Modules~~

Type	Layers 1 oz	Function	Die #	Type	Package	Package Size (mm x mm)	Die Size (mm x mm)	Via Array (mm x mm)	Via Pitch (mm)
2230	4 ~~1 oz~~	WiFi/BT	1	WiFi/BT	QFN	9x9	6x6	6x6	1
3042	8 ~~1 oz~~	WWAN	1	Baseband	PBGA	10x10	5.5x5.5	4x4	1.27
			2	Power Mgmt.	PBGA	4x4	2x2	2x2	1.27
			3	RF Transceiver	PBGA	5x5	3x3	2x2	1.27
			4	PA	LGA	5x7	1.3x2	2x6	1
2280 Double-sided	6 ~~1 oz~~	SSD	1	ASIC	BGA	20x20	12x12	9x9	1.27
			2	DRAM	BGA	11x10	7x7		
			3	NAND1	BGA	15x18	10x12		
			4	NAND2	BGA	15x18	10x12		
			5	NAND3	BGA	15x18	10x12		
			6	NAND4	BGA	15x18	10x12		
			7	POWER	DFN	6x5	4.125x3.75		
3030	6 ~~1 oz~~		1	WiFi/BT	QFN	9x9	6x6	6x6	1

		Wi-Fi/BT + Wi-Gig	2	Wi-Gig	PBGA	9x9	6x6	4x4	1.27

6.5.2. Generic System Environment Categories (Assumptions)

Table 61 gives assumptions for each generic system environment. These are meant to be slightly aggressive targets at the time of writing.

Table 61. Assumptions for Generic System Environments

Type	Notebook		Thin ~~Platform~~Platform Notebook With Fan		Tablet Fanless	Units
Case Size	325 x 225		325 x 225 (14”)		250 x 170	
Total /Base Thickness	28/18		15/10		8	mm
Case Material	Resin		Mg		Mg	
Case Thickness	1.1		0.8		0.8	mm
Case Exterior Emissivity	High		High		High	
Case Interior Emissivity	High		Low		Low	
External Ambient	25	35 (see Note 1)	25	35 (see Note 1)	25	°C
Skin T Limit Top (“Forehead”)	37	55	37	46	40 (display)	°C
Skin T Limit Bottom	48	58	42	46	38	°C
Gap Adapter ~~Module~~ to Case	> 2		> 1		< 0.5	mm
~~Motherboard~~Motherboard Size	180 x 83 x 1.2		180 x 83 x 1		140 x 45 x 0.9	mm
Adapter ~~Module~~ Orientation	Table		Table		Back	
Inlet Vent Area	30 x 30 + 83 x 16 + 2 edge vents 20 x 2.5		60 x 30 + 2 edge vents 20 x 5		N/A	
Outlet Vent Area	60 x 10 grille		60 x 10 grille		N/A	mm
Fan Flow Rate	2.4 ~~cfm~~ 68 ~~l/min~~		0.6 ~~cfm~~ 17 ~~l/min~~		N/A	cfm (see Note 2) lpm (see Note 3)

Notes:

1. Shown for example purposes only
2. Cubic feet per minute
3. Liter per minute

6.5.2.1. Adapter ~~Module~~ Slot Definitions by System

The following assumptions apply to the results and discussions of the examples in this document.

- 25 °C ambient is assumed for skin temperature compliance
- Socket 1 = Wi-Fi/BT OR Wi-Fi/Wi-Gig
- Socket 2 = WWAN
- Socket 3 if present = SSD
- Wi-Fi/BT and WWAN operation are **mutually exclusive**; i.e.,~~i.e.~~ the system is connected to one or the other, but not both
- If socket 3 is present, socket 2 is WWAN
- Skin temperature limits are OEM dependent and sometimes market sector dependent
- Global skin temperature levels are system dependent (heat exchanger design, fan flow rate, board layout, system TDP distribution)
- Local skin temperatures and Adapter ~~module~~ TDP values are given assuming no special thermal management techniques have been applied to either the Adapter ~~module~~ or the nearby casing
- Thermally advantageous placement of Adapter ~~modules~~ is assumed

6.5.2.1.1. Systems with Fans

Table 62. Slot Definitions, Systems with Fans

	Notebook		**Thin ~~Platform~~Platform Notebook ~~With~~ with Fan**		
Socket #	1	2	1	2	3
Adapter ~~Module~~ Size	2230	3042	3030	3042	2280
Function	Wi-Fi/BT	WWAN	Wi-Fi/BT + Wi-Gig	WWAN	SSD

6.5.2.1.2. Systems without Fans

Table 63. Slot Definitions, Systems without Fans

	Tablet	
Scenario		
Socket #	1	2
Adapter ~~Module~~ Size	2230	3042
Function	Wi-Fi/BT	WWAN LTE

6.5.3. Assessing Thermal Design Power Capability

6.5.3.1. Use Cases

Assumptions for the distribution of thermal dissipation throughout the system are needed for each system type. These are known as “use cases” and are established by defining a scenario for what the user is asking the system to do. In many cases, there are simultaneous active applications taxing different areas of the system. The use cases in this document are intended for illustration only; an analogous process should be carried out by system designers for each system.

6.5.3.2. Extended Use Cases

To evaluate system and Adapter ~~module~~ response to TDP variations, a use case baseline is established, and the Adapter ~~module~~ dissipation varied around the nominal value for the use case. In this document, the “extended use case” (the use case plus a higher dissipation for the Adapter ~~module~~ in question) is analyzed for skin temperature response. Hypothetical example systems are modeled with use cases relevant to dissipation in the Adapters~~modules~~. The Adapter ~~module~~ dissipation is varied over the range 0 – use case TDP – 3 W to obtain the sensitivity of skin temperature to Adapter ~~module~~ dissipation.

6.5.3.3. Unpowered Adapter ~~Module~~

For Adapter ~~module~~ designers, the use cases are valuable background to establishing potential Adapter ~~module~~ environments. Particularly helpful for them should be the system skin and module temperatures when there is an **unpowered** Adapter ~~module~~, which is meant to give an idea of the starting point for any thermal excursion due to the Adapter’s ~~module’s~~ own power.

6.5.3.4. Use Case Flexibility

It is worthwhile to note that in some instances, the stated assumptions about use case do not result in a system that meets its specifications. Including power management features in the Adapter ~~module~~ components will give system designers maximum flexibility to manage power dissipation. This flexibility ~~can be~~ applies~~d~~ to many of the system’s components to meet specifications. It should be noted again that for skin temperature limits, the time scale of interest is of the order of several minutes, while the time scale for many system tasks is much shorter.

Most business applications enable the wireless communications Adapters ~~modules~~ to go dormant, thereby lowering the average thermal dissipation. Applications that perform data streaming such as VOIP, video streaming from an attached camera or streaming audio prevent the communications Adapters ~~modules~~ from going dormant. The host should support the USB Selective Suspend feature to reduce electrical power consumption and thermal dissipation by the wireless Adapters~~modules~~.

6.5.4. Adapter ~~Module~~ Placement Advice

Lowest skin temperatures will be achieved when the heat sources are distributed over the largest possible area. This implies that, within reason, the Adapters ~~modules~~ should be located away from areas of concentrated heat on the ~~motherboard~~motherboard, and also as far as possible from any heat exchanger.

For systems with fans, place inlet vents near Adapters ~~modules~~ to flush the inside surface of the casing, and use the bottom vent to act as a thermal break if needed.

Address global hot spots via general system layout and use case assumptions.

6.5.5. Skin Temperature Sensitivity to Adapter ~~Module~~ Power

Skin temperatures in the vicinity of Adapters ~~modules~~ will depend on the Adapter ~~module~~ power and the total system power and its arrangement. Systems with low flow rates will have higher sensitivity than systems with higher flow rates. Systems without ventilation are most sensitive, up to 3 °C skin temperature increase per Watt of Adapter ~~module~~ power in the example systems shown in Appendix A~~the Appendix~~. This value may not be generally applicable – thermal studies should be carried out at the system level.

6.5.6. General Applicability

The examples shown in section 6.5.8, *Examples*, are not intended to be generally applicable. They are only meant to show the potential range of responses, and to determine sensible advice for Adapter ~~module~~ placement and other approaches to thermal management. The TDP response has to be established by the design team for each system design. Thermal analysis by computational and physical (experimental) modeling is strongly encouraged at the system level.

6.5.7. Generic Assumptions for Adapter ~~Module~~ Arrangement

Adapters ~~Modules~~ may represent a significant portion of the total system dissipation and may be a major contributor to system skin temperature. It is a good idea to place them in thermally advantageous locations. Examples shown throughout this document indicate such thermally advantageous placements, but of course are only meant to show the possibilities, and do not represent actual final designs. Nor have all the model assumptions been completely tested, so the accuracy of any predictions is within several degrees at best.

For systems with fans, vents upstream help to cool both the Adapter ~~module~~ and the nearby casing to minimize skin temperature. They may also have a "thermal break" effect, protecting the local surface near the Adapters ~~modules~~ from the larger global maximum surface temperature.

For systems without fans, concentrations of high heat density should be avoided~~as a matter of course~~, since the thin metal skin ~~can~~ achieves only a limited level of heat spreading. In addition, it is

well known that placing heat sources near edges or corners of a heat spreader cause higher temperatures than placing them in a central location on the spreader.

6.5.8. Examples

6.5.8.1. Notebook Category

Many assumptions are used in this document. Table 64 lists examples of cases applicable to Adapters ~~modules~~ for notebooks.

Table 64. Example Use Case Applicable to Adapters ~~Modules~~ for Notebooks

Component	**~~Thermal Design Power~~TDP (W)**
Scenario	Comms Excursion
Application Mix	Local Network (WiFi) File Transfer+ Device (BT) File Copy+ Netflix (Chrome) 1080p [+WiF~~D~~i]
~~Motherboard~~Motherboard CPU	26
~~Motherboard~~Motherboard VR, chipset, etc.	8.2
Memory	1.5
HDD+SSD Cache	1.1
HDD	0.1
SSD Cache	1.0
Comms: WLAN/BT	2.2
Comms: WWAN	0.0
ODD	0.1
Fan	0.9
~~Platform~~Platform Total	**40**

6.5.8.1.1. Generic ~~Motherboard~~Motherboard Assumptions

The bottom view of a single-sided ~~motherboard~~motherboard (all components facing the table within the system) with a thermal solution applied to CPU is shown in Figure 133. The Adapters ~~modules~~ are installed in top mount connectors at one edge of the board, as far from the CPU as possible. There are several memory Adapters ~~modules~~ and two areas of clustered small heat sources, each shown as a rectangular heated area. The ~~motherboard~~motherboard heat sources form a thermal boundary condition for the Adapters ~~modules~~.

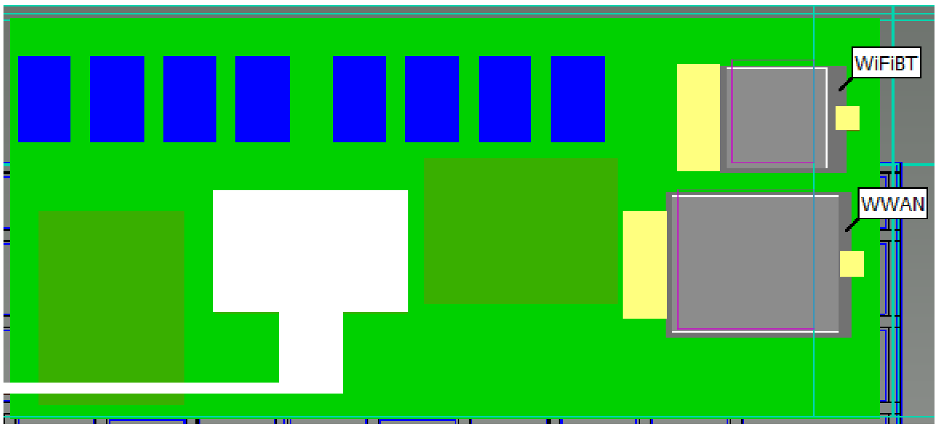


Figure 133. Example View of Notebook ~~Motherboard~~Motherboard

6.5.8.1.2. System Layout Assumptions

Flow related assumptions include a fan at ~~2.4 cfm/~~68 ~~l~~l/min (2.4 cfm), a vent opening near the cards, and small slot vents in the system's side (Figure 134 shows edge vents and Figure 135 shows bottom vents).

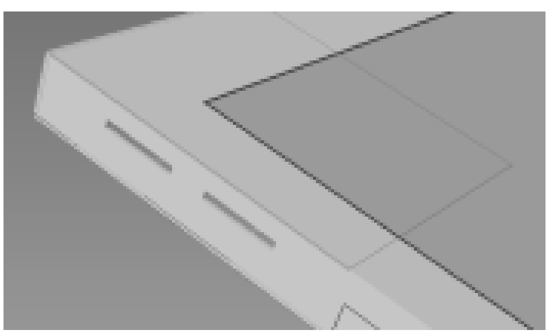


Figure 134. Example View of Edge Vents

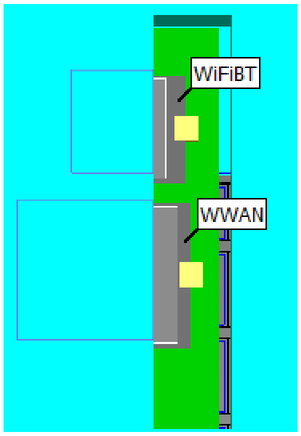


Figure 135. Example View of Bottom Vents (vent opening where inside boards are visible through the opening)

6.5.8.1.3. Local Skin Temperature

Since temperature varies continuously over the surface of the system, locating the point of interest for surface temperature measurement consistently is very important. For a global maximum, identification is straightforward in a thermal model or by infrared camera in a physical model. For a notebook system, the global maximum is likely to be near the heat exchanger and fan exhaust. The temperature in this region is only very slightly dependent on the Adapter ~~module~~ dissipation, as in this system category the Adapter ~~module~~ makes up a relatively small fraction of the total system TDP.

Local maxima are trickier to identify if they are lower than the global maximum. For the purposes of the examples shown in Figure 136 and Figure 137, a region of interest is defined in the vicinity of the Adapters ~~modules~~, and the region maximum obtained. Another method might be to track a single consistent point over each Adapter~~module~~.

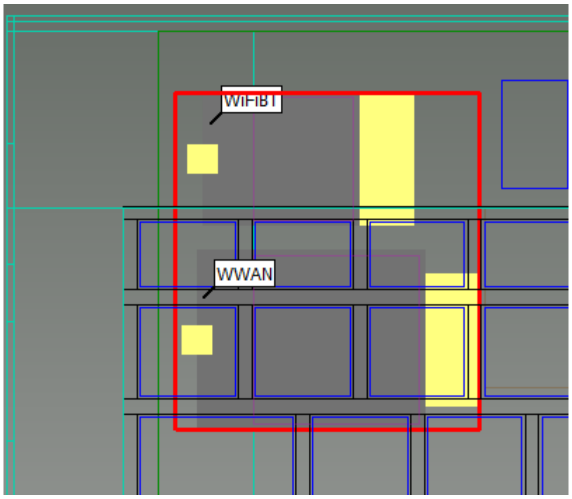


Figure 136. Example View of Region Over Adapters ~~Modules~~

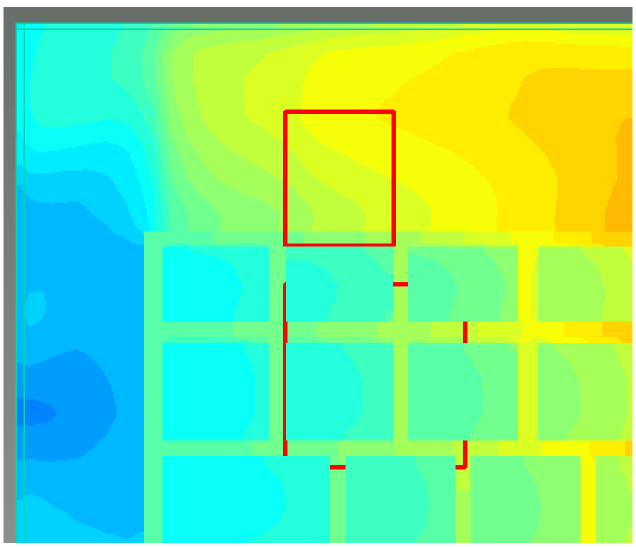


Figure 137. Example View of Hot Spot Over Adapters ~~Modules~~

6.5.8.1.4. Thermal Design Power Response – Notebook Category

The models were run at three powers for each card – zero, nominal per use case, and "extended" to 3 W in the use case. Results are shown in Table 65, Table 66, and Table 67. Temperatures are rounded to the nearest whole degree.

Note that the table distinguishes between local skin temperature (directly over or under the Adapter~~module~~) and a global skin hot spot, caused by the remainder of the system and use case, sometimes even in the absence of any Adapter ~~module~~ dissipation. Although the Adapters ~~modules~~ do not heat the skin excessively, the system designer will have to consider changes in the use case and/or the design to meet skin temperature requirements.

Also note that with so many assumptions in each analysis, the results shown in the table are not intended as accurate predictions, but only to provide guidance about sensible system design for Adapter ~~module~~ effects on skin temperature. The particulars of the keyboard model especially determine the skin temperature of Adapters ~~modules~~ below the keyboard area.

Table 65. Thermal Design Power Response – Notebook Category

	Notebook	Notebook	Units
Socket #	1	2	
Adapter ~~Module~~ Size	2230	3042	
Function	WiFi/BT	WWAN	
Use case	Comms Exc	Comms Exc WWAN	
System Dissipation W/O Adapter~~Module~~	37.8	37.8	W
Adapter ~~Module~~ Off	0 ~~W~~	0 ~~W~~	W
Mean Card T	32	34	°C
Local Skin T Top	30	28	°C
Local Skin T Bottom	28	30	°C
Global Skin Hot Spot (HX)	47	47	°C
Use Case TDP	2.2 ~~W~~	2.2 ~~W~~	W
Local Skin T Top	31	28	°C
Local Skin T Bottom	30	31	°C
Global Skin Hot Spot (HX)	47	47	°C
Extended Case TDP	3 ~~W~~	3 ~~W~~	W
Local Skin T Top	31	29	°C
Local Skin T Bottom	31	31	°C
Fan Flow Rate~~, CFM~~	2.4	2.4	cfm

Table 66. Skin Temperature Limit Assumptions, Notebook

	Value	Units
Ext Ambient	25	~~25~~°C
Skin T Limit Top	37	~~37~~°C
Skin T Limit Bottom	48	~~48~~°C

Table 67. Skin Temperature Effect of Adapter ~~Module~~ Position

Adapter ~~Modules~~ Switched Places	Notebook		Units
Socket #	1	2	
Adapter ~~Module~~ Size	3042	2230	
Function	WWAN	WiFi/BT	
Use Case	Comms exc WWAN	Comms exc	
Use Case TDP	2.2	2.2	W
Local Skin T Top	28	31	°C
Local Skin T Bottom	31	30	°C

6.5.8.2. Thin ~~Platform~~Platform Notebook with Fan Category

Many assumptions are used in this document. Table 68 shows the use cases applicable to Adapters ~~modules~~ for thin ~~Platform~~Platform notebook with fan.

Table 68. Use Cases Applicable to Adapters ~~Modules~~ for Thin ~~Platform~~Platform Notebook with Fan

Component	Thermal Design Power (W) by Scenario	
Scenario	~~Platform~~Platform Chipset Excursion	Comms Excursion
Application Mix	Skype+ Windows Media Player+ OS File Transfers+ SS Storage File Copy	Local Network (WiFi) File Transfer+ Device (BT) File Copy+ Netflix(Chrome) 1080p [+WiDi]
~~Motherboard~~Motherboard CPU ~~-~~ + Chipset	13.5	12.8
~~Motherboard~~Motherboard Distributed	4.2	3.7
Memory	1.5	1.5
SSD	2.4	0.5
Comms: ~~-~~WLAN/BT or WWAN	0.9	1.4
~~Platform~~Platform Total	23.4	20.8

6.5.8.2.1. Generic ~~Motherboard~~Motherboard Assumptions

The bottom view of a single-sided ~~motherboard~~motherboard (all components facing the table within the system) with thermal solution applied to CPU is shown in Figure 138. The cards are installed in mid-mount connectors at one edge of the board, as far from the CPU as possible. There are several memory Adapters ~~modules~~ and two areas of clustered small heat sources, each shown as a rectangular heated area. The ~~motherboard~~motherboard heat sources form a thermal boundary condition for the Adapters~~modules~~.

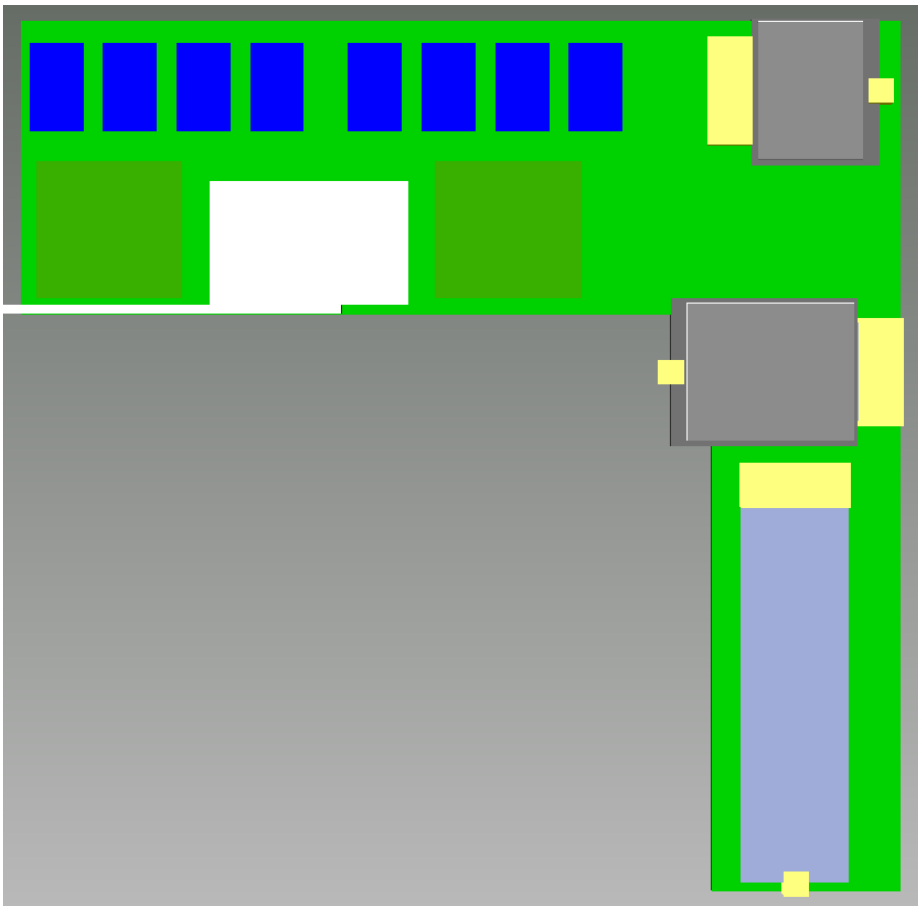


Figure 138. Example View of ~~Motherboard~~Motherboard for Thin ~~Platform~~Platform Notebook with Fan

6.5.8.2.2. System Layout Assumptions

Flow related assumptions include a fan at ~~0.6 cfm/~~17 ~~l~~l/min (0.6 cfm), a vent opening below the Adapters~~modules~~, and small slot vents in the system's side (see Figure 139). The vent opening below the cards ~~can~~ reduces the local surface temperature.

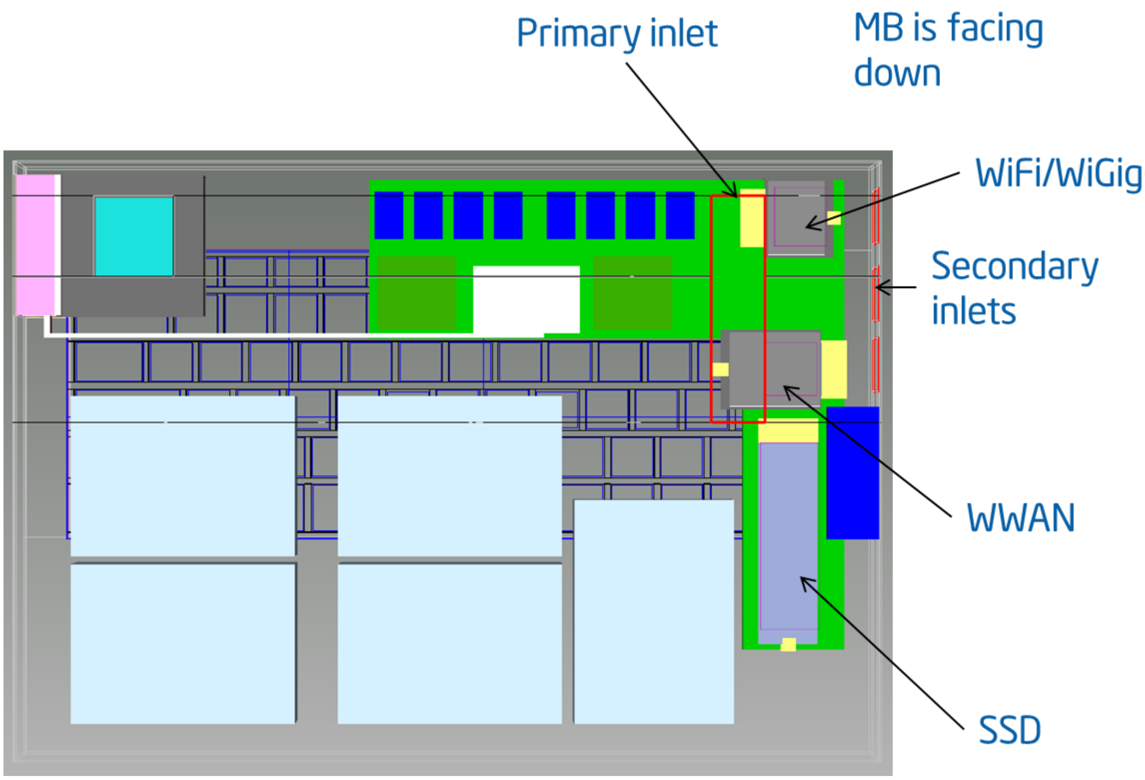


Figure 139. Thin ~~Platform~~Platform Notebook Layout with Vents and Key Components

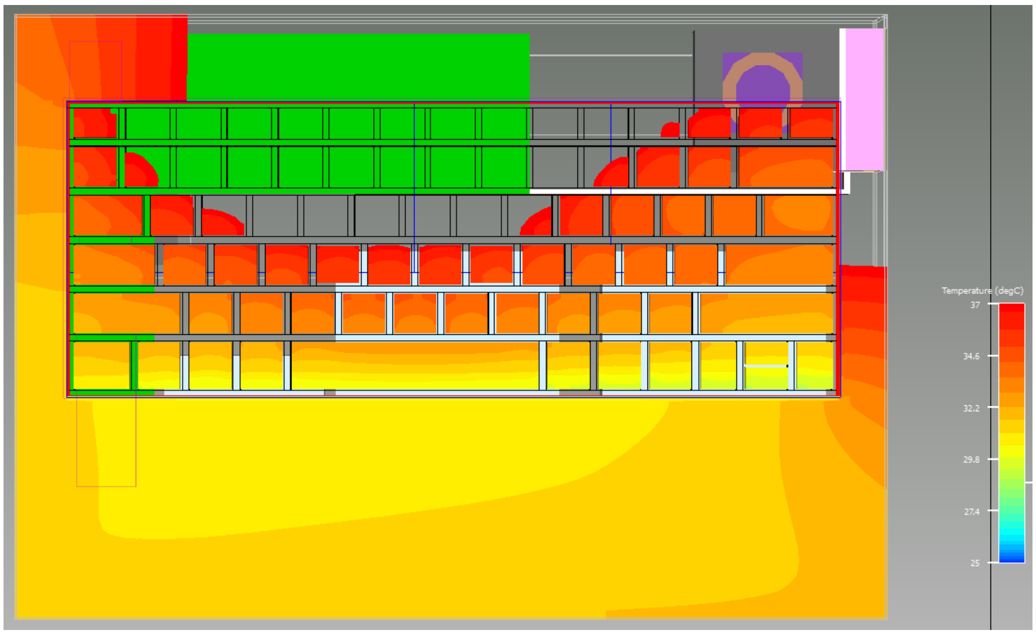
6.5.8.2.3. Adapter ~~Module~~ Placement Advice – Thin ~~Platform~~Platform Notebook

Lowest skin temperatures will be achieved when the heat sources are distributed over the largest possible area. This implies that, within reason, the Adapters ~~modules~~ should be located away from areas of concentrated heat on the ~~motherboard~~motherboard, and especially as far as possible from the heat exchanger. Place inlet vents near Adapters ~~modules~~ to flush the inside surface of the casing, and use the bottom vent to act as a thermal break if needed. Address global hot spots via general system layout and use case assumptions.

6.5.8.2.4. Local Skin Temperature

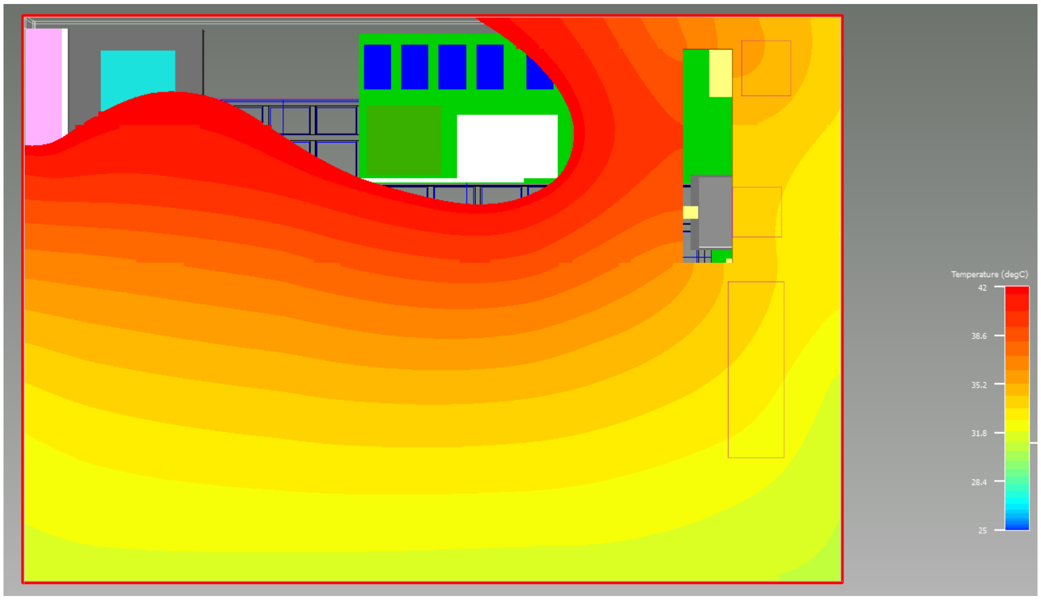
Since temperature varies continuously over the surface of the system, locating the point of interest for surface temperature measurement consistently is very important. For a global maximum, identification is straightforward in a thermal model or by infrared camera in a physical model. For a notebook system, the global maximum is likely to be near the heat exchanger and fan exhaust. The temperature in this region is somewhat dependent on the Adapter ~~module~~ dissipation~~, as in this system category is makes up a meaningful fraction of the total system TDP~~. In addition, the fan flow rate is quite low, so that the casing needs to transfer a larger fraction of the total heat.

Local maxima are trickier to identify if they are lower than the global maximum. For the purposes of the examples shown in Figure 140 and Figure 141, a region of interest is defined in the vicinity of the Adapters~~modules~~, and the region maximum obtained. Another method might be to track a single consistent point over each Adapter~~module~~.



- Rectangles indicate local card areas~~;~~
- Irregularly unshaded areas indicate surface above the maximum scale temperature
- Note scale corresponds to maximum skin temperature assumptions

Figure 140. Example View of Region and Hot Spots Over Adapters~~Modules~~



- Rectangles indicate local card areas~~;~~
- Irregularly unshaded areas indicate surface above the maximum scale temperature
- Note scale corresponds to max skin temperature assumptions

Figure 141. Example View of Region and Hot Spots Under Adapters~~Modules~~

6.5.8.2.5. Thermal design Power Response – Thin ~~Platform~~Platform Notebook with Fan Category

The models were run at three powers for each card – zero, nominal per use case, and "extended" to ~3+ W in the use case. The results in Table 69 and Table 70 are model predictions at zero and at the extended use case, to bracket expectations. Temperatures are rounded to the nearest whole degree.

Note that the table distinguishes between local skin temperature (directly over or under the Adapter~~module~~) and a global skin hot spot, caused by the remainder of the system and use case, sometimes even in the absence of any Adapter ~~module~~ dissipation. Although the Adapters ~~modules~~ do not heat the skin excessively, the system designer will have to consider changes in the use case and/or the design to meet skin temperature requirements.

Also note that with so many assumptions in each analysis, the results shown in the table are not intended as accurate predictions, but only to provide an example of Adapter ~~module~~ effects on skin temperature. The flow rate of the fan and particulars of the keyboard model especially determine the skin temperature of Adapters ~~modules~~ below the keyboard area.

Table 69. Thermal Design Power Response – Thin ~~Platform~~Platform Notebook with Fan Category

	Thin ~~Platform~~Platform Notebook with Fan				Units
Socket #	1	1	2	3	
Adapter ~~Module~~ Size	3030	3030	3042	2280	
Function	WiFi/BT + WiGig	WiFi/BT + WiGig	WWAN	SSD	
Use Case	Comms exc	Comms exc 50% power	Comms exc WWAN	~~Platform~~Platform Chipset exc	
Sys Dissipation W/O Adapter~~Module~~	19.4	9.7	19.4	21	W
Adapter ~~Module~~ Off	0 ~~W~~	0 ~~W~~	0 ~~W~~	0 ~~W~~	W
WMean Card T	42	31	38	33	°C
Local Skin T Top	33	29	34	32	°C
Local Skin T Bottom	32	29	32	33	°C
Global Skin Hot Spot (HX)	46	36	47	47	°C
Use Case TDP	1.4 ~~W~~	0.7 ~~W~~	1.4 ~~W~~	2.4 ~~W~~	W
Local Skin T Top	35	30	39	37	°C
Local Skin T Bottom	36	30	36	38	°C
Global Skin Hot Spot	47	37	48	49	°C
Extended Case TDP	3 ~~W~~	3 ~~W~~	3 ~~W~~	3 ~~W~~	W
Local Skin T Top	38	35	41	39	°C
Local Skin T Bottom	38	36	37	39	°C
Fan Flow Rate~~, Cfm~~	0.6	0.6	0.6	0.6	cfm

Table 70. Skin T~~t~~emperature L~~l~~imit A~~a~~ssumptions, Thin P~~p~~latform N~~n~~otebook with Fan

	Value	**Units**
Ext Ambient	25	~~25~~°C
Skin T Limit Top	37	~~37~~°C
Skin T Limit Bottom	42	~~42~~°C

6.5.8.3. Tablet without Fan Category

Many assumptions are used in this document. Table 71 lists the use cases applicable to Adapters ~~modules~~ for tablet without fan.

Table 71. Use Cases Applicable to Adapters ~~Modules~~ for Tablet without Fan

Component Dissipation (W)	Estimate I Skype—Over 3G Steady State	Estimate II Skype + 19x10 Display + 3G	Units
SOC Package	1.16	1.5	W
POP Memory (2 GB)	0.29	0.4	W
3G Comms	0.80	1.4	W
Camera	--	0.25	W
Storage (eMMC)	0.05	--	W
PMIC	0.86	0.7	W
Audio LPE	0.05	0.1	W
MIPI to LVDS	0.13	--	W
Display (10”, 200 nits)	2.46	1.935	W
Battery Discharge	0.14	0.1	W
Others (system VR, LEDs, etc.)	0.43	0.1	W
~~Platform~~Platform Total	6.37	6.485	W

6.5.8.3.1. Generic ~~Motherboard~~Motherboard Assumptions

The bottom view of a single-sided ~~motherboard~~motherboard (all components facing the back within the system) is shown in Figure 142. The cards are installed in Mid-mount connectors at one edge of the U-shaped board. There are several memory Adapters~~modules~~, a power management IC (PMIC), and two areas of clustered individual small heat sources (each shown as a rectangular heated area). The ~~motherboard~~motherboard heat sources form a thermal boundary condition for the Adapters~~modules~~.

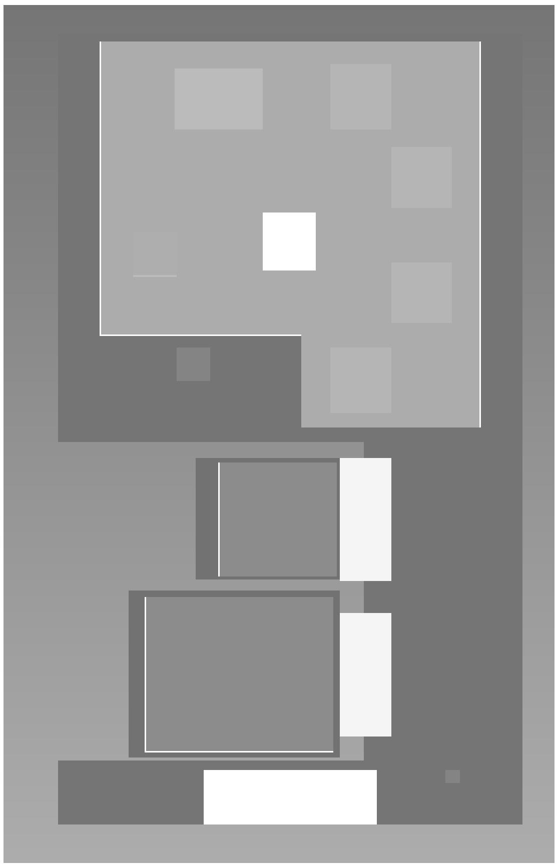


Figure 142. Example View of Tablet ~~Motherboard~~Motherboard

6.5.8.3.2. System Layout Assumptions

It is assumed that there is neither a fan nor venting in a tablet—a high emissivity surface has been assumed on the outside surface of the magnesium enclosure. In addition, the heat spreader under the backlight assembly is 0.2 mm thick copper since copper will reduce the hot spot compared to an aluminum spreader.

The ~~motherboard~~motherboard is centrally located, between banks of batteries. This arrangement allows the heat to spread in all directions; concentrating heat sources in a corner restricts their heat spreading ability (see Figure 143).

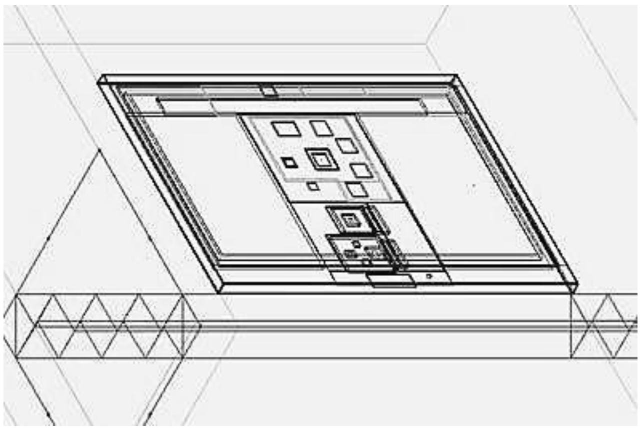


Figure 143. Example View of System Layout, Including Table

6.5.8.3.3. Local Skin Temperature

Since temperature varies continuously over the surface of the system, locating the point of interest for surface temperature measurement consistently is very important. For a global maximum, identification is straightforward in a thermal model or by infrared camera in a physical model. The global maximum is likely to be over the main dies (SoC and PMIC). The temperature in this region is somewhat dependent on the Adapter ~~module~~ dissipation, as in this system category it makes up a significant fraction of the total system TDP. As there is no flow at all, the casing needs to transfer all the heat dissipated inside (see Figure 144 and Table 72).

Local maxima are trickier to identify if they are lower than the global maximum. The global maximum point was chosen because with no ventilation possible, any hot spots interact; all heat must spread and dissipate off the surface.

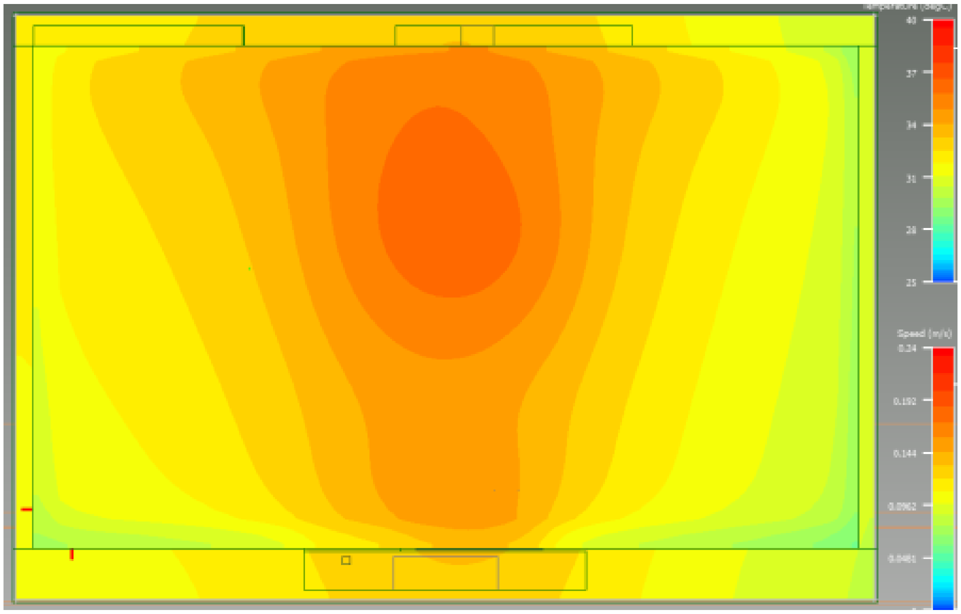


Figure 144. Example View of Display Surface Temperature with WWAN Use Case Estimate II

Table 72. Thermal Design Power Response—Tablet Category

	Tablet		Units
Socket #	1	2	
Adapter ~~Module~~ Size	2230	3042	
Function	WiFi/BT	WWAN LTE	
Use Case	Estimate II		
Sys Dissipation W/O ~~Mod~~Adapter~~ule~~	5.1	5.1	W
Adapter ~~Module~~ Off	0 ~~W~~	0 ~~W~~	W
Mean Card T	31	31	°C
Local Display T	35	35	°C
Max Back T	32	32	°C
Use Case TDP	1.4 ~~W~~	1.4 ~~W~~	W
Local Display T	37	37	°C
Max Back T	34	34	W
Extended Case TDP	3 ~~W~~	3 ~~W~~	W
Local Display T	39	38	°C

Max Back T	39	37	°C

6.5.8.3.4. Thermal Design Power Response—Tablet Category

The models were run at three powers for each card – zero, nominal per use case, and “extended” to ~3+ W in the use case. Results in the table are model predictions at zero and at the extended use case, to bracket expectations. Temperatures are rounded to the nearest whole degree Celsius.

Also note that with so many assumptions in each analysis, the results shown in Table 73 are not intended as accurate predictions, but only to provide an example of Adapter ~~module~~ dissipation effects on skin temperature.

Table 73. Skin Temperature Limit Assumptions, Tablet without Fan

Ext Ambient	Skin T Limit Display	Skin T Limit Back	Units
25	40	38	°C

6.6. Examples of FULL_CARD_POWER_OFF# Sequences (Informative)

6.6.1. Example of Power On/Off Sequence

Following is an example of a full-card power On/Off sequence:

1. Modem power on:
   High level will trigger modem power on sequence.
2. Modem power off:
   The modem is powered off first via an AT command, subsequently there is a handshaking between host and modem.
3. FULL_CARD_POWER_OFF# pin will turn to LOW level or Tri-state to shutdown modem’s PMU.

6.6.2. Example of Tablet Power On/Off Sequence

The following example sequences are for illustrative purposes only, as Adapter ~~module~~ vendors ~~can~~ offers alternate solutions and requirements.

1. Battery always connected to modem.
2. Host triggers GPIO to High on the FULL_CARD_POWER_OFF# pin.
3. Modem turns On.
4. Host issue AT command to switch off modem.
5. Handshaking between modem and host.

6. Host sets GPIO to LOW (or Tri-state) on FULL_CARD_POWER_OFF# pin which will switch off modem PMU.

Following is the proper Shutdown Handshaking Process.

1. PC Host sends AT+CFUN=0 to Modem.
2. Modem responds OK.
   Modem will do the essential shutdown tasks before sending OK:
   a) Proper detaching from cellular network.
   b) SW clean up functions, saving necessary NVM parameters and etc.
   c) Activate SIM/EBU shutdown sequences.
   d) Above task may need few milliseconds to couple of seconds depending on the state of the modem.
3. Modem sends OK to AP upon completion of essential tasks.
4. If AP receives ERROR, it should try again for AT+CFUN=0.
5. Modem completes PMU power off sequences/register access after sending OK.
   The following process takes less than one second:
   a) Disable all regulators (except VPMU and VRTC LDOs).
   b) Assert reset signals.
   c) Release the 26 MHz system clock request signal.
6. AP cuts off power supply or pull-on/off pin LOW /Tri-state after fixed delay of one second.
   In a rare case, if AP did not receive any response within _*_ seconds of issuing AT+CFUN=0, AP will assume that it is OK. There may be times when USB may be over loaded and by the time it is ready to send OK, the driver shutdown will already have started and OK may not reach AP.

> **Note:** *The response time _*_ is to be decided by the host.

6.6.3. Example of Very T~~-t~~hin Notebooks Power On/Off Sequence

Very t~~-t~~hin notebooks do not use the FULL_CARD_POWER_OFF# signal. Following is the power ON/Off sequence example for very t~~-t~~hin notebooks:

1. Modem gets 3.3 V once the ~~Platform~~Platform switches on the 3.3 V Always On supply for the modem.
2. Modem turns On since the FULL_CARD_POWER_OFF# pin is pulled high by the host (pin 6 connected to 1.8 V or 3.3 V).
3. Host issues AT command to switch off modem.
4. Handshaking between modem and host. Once the handshake has been complete, the host ~~can~~ is permitted to shut off supply to the modem.

6.7. Socket 2 Key C - Vendor Defined Pinout Examples

Table 74 ~~Table 74~~ lists examples of Vendor Defined pinouts.

Table 74. Socket 2 Key C - Vendor Defined Pinout Examples

Pin	Pin Name in Pinout	Generic Example	Example 1	Example 2
63	VENDOR_PORT_C_3 (Top)	VENDOR DEFINED (I/O) (0/1.8V)	AUDIO2 I2S_WS (I/O) (0/1.8V)	IPC_5 (I/O) (0/1.8V)
61	VENDOR_PORT_C_2 (Top)	VENDOR DEFINED (I/O) (0/1.8V)	AUDIO1 I2S_TX (O) (0/1.8V)	SERIAL S/B DATA_TX (O) (0/1.8V)
57	VENDOR_PORT_C_1 (Top)	VENDOR DEFINED (I/O) (0/1.8V)	AUDIO1 I2S_RX (I) SLIMBUS_DAT (I/O) (0/1.8V)	SERIAL S/B DATA_RX (I) (0/1.8V)
55	VENDOR_PORT_C_0 (Top)	VENDOR DEFINED (I/O) (0/1.8V)	AUDIO1 I2S_CLK (I/O) SLIMBUS_CLK (I/O) (0/1.8V)	SERIAL S/B CLK (I) (0/1.8V)
60	VENDOR_PORT_B_5 (Bottom)	VENDOR DEFINED (I/O) (0/1.8V)	FINE TIME ADJUSTMENT (O) (0/1.8V)	IPC_7 (I/O) (0/1.8V)
58	VENDOR_PORT_B_4 (Bottom)	VENDOR DEFINED (I/O) (0/1.8V)	TX_BLANKING (O) (0/1.8V)	IPC_6 (I/O) (0/1.8V)
54	VENDOR_PORT_B_3 (Bottom)	VENDOR DEFINED (I/O) (0/1.8V)	SYSCLK (O) (0/1.8V)	IPC_4 (I/O) (0/1.8V)
52	VENDOR_PORT_B_2 (Bottom)	VENDOR DEFINED (I/O) (0/1.8V)	GNSS_IRQ (O) (0/1.8V)	IPC_3 (I/O) (0/1.8V)
50	VENDOR_PORT_B_1 (Bottom)	VENDOR DEFINED (I/O) (0/1.8V)	GNSS_SDA (I/O) (0/1.8V)	IPC_2 (I/O) (0/1.8V)
48	VENDOR_PORT_B_0 (Bottom)	VENDOR DEFINED (I/O) (0/1.8V)	GNSS_SCL (I) (0/1.8V)	IPC_1 (I/O) (0/1.8V)
14	VENDOR_PORT_A_3 (Bottom)	VENDOR DEFINED (I/O) (0/1.8V)	HOST-WAKE# (I) (0/1.8V)	HOST-WAKE# (I) (0/1.8V)
12	VENDOR_PORT_A_2 (Bottom)	VENDOR DEFINED (I/O) (0/1.8V)	WoWWAN# (O) (0/1.8V)	WoWWAN# (O) (0/1.8V)
10	VENDOR_PORT_A_1 (Bottom)	VENDOR DEFINED (I/O) (0/1.8V)	LED_1# (O) (OD)	VENDOR DEFINED (I/O) (0/1.8V)
8	VENDOR_PORT_A_0 (Bottom)	VENDOR DEFINED (I/O) (0/1.8V)	W_DISABLE# (I) (0/1.8V)	IPC_0 (I/O) (0/1.8V)

Pin	Pin Name in Pinout	Example 3	Example 4	Example 5
63	VENDOR_PORT_C_3 (Top)	UART_TX (O) (0/1.8V)	#2 M/PERp0; SSIC RxP;USB3.1-Rx+	#2 M/PERp0; SSIC RxP;USB3.1-Rx+
61	VENDOR_PORT_C_2 (Top)	UART_RTS (O) (0/1.8V)	#2 M/PERn0; SSIC RxN; USB3.1-Rx-	#2 M/PERn0; SSIC RxN; USB3.1-Rx-
57	VENDOR_PORT_C_1 (Top)	UART_RX (I) (0/1.8V)	#2 M/PETp0; SSIC TxP;USB3.1-Tx+	#2 M/PETp0; SSIC TxP;USB3.1-Tx+
55	VENDOR_PORT_C_0 (Top)	UART_CTS (I) (0/1.8V)	#2 M/PETn0; SSIC TxN;USB3.1-Tx-	#2 M/PETn0; SSIC TxN;USB3.1-Tx-
60	VENDOR_PORT_B_5 (Bottom)	FINE TIME ADJUSTMENT (O) (0/1.8V)	FINE TIME ADJUSTMENT (O) (0/1.8V)	#2 M/REFCLKP
58	VENDOR_PORT_B_4 (Bottom)	TX_BLANKING (O) (0/1.8V)	TX_BLANKING (O) (0/1.8V)	#2 M/REFCLKN
54	VENDOR_PORT_B_3 (Bottom)	SYSCLK (O) (0/1.8V)	SYSCLK (O) (0/1.8V)	PEWAKE# (I/O) (0/1.8V)
52	VENDOR_PORT_B_2 (Bottom)	GNSS_IRQ (O) (0/1.8V)	GNSS_IRQ (O) (0/1.8V)	CLKREQ# (I/O) (0/1.8V)
50	VENDOR_PORT_B_1 (Bottom)	GNSS_SDA (I/O) (0/1.8V)	GNSS_SDA (I/O) (0/1.8V)	PERST# (I) (0/1.8V)
48	VENDOR_PORT_B_0 (Bottom)	GNSS_SCL (I) (0/1.8V)	GNSS_SCL (I) (0/1.8V)	SERIAL S/B CLK (I) (0/1.8V)
14	VENDOR_PORT_A_3 (Bottom)	HOST-WAKE# (I) (0/1.8V)	HOST-WAKE# (I) (0/1.8V)	HOST-WAKE# (I) (0/1.8V)
12	VENDOR_PORT_A-2 (Bottom)	WoWWAN# (O) (0/1.8V)	WoWWAN# (O) (0/1.8V)	WoWWAN# (O) (0/1.8V)
10	VENDOR_PORT_A_1 (Bottom)	LED_1# (O) (OD)	LED_1# (O) (OD)	SERIAL S/B DATA_TX (O) (0/1.8V)
8	VENDOR_PORT_AB_0 (Bottom)	W_DISABLE# (I) (0/1.8V)	W_DISABLE# (I) (0/1.8V)	SERIAL S/B DATA_RX (I) (0/1.8V)

6.8. High Speed Differential Pair AC Coupling Cap Values and Cap Location Examples

This chapter will summarize the defined High Speed Differential Pair AC Coupling Cap values and illustrate examples of where the AC Coupling Caps should be located based on the definitions outlined in the following document:

- *~~PCIe~~ PCI Express Base Specification*
- *PCI Express Card Electromechanical (CEM) Specification*
- *Universal Serial Bus Specification, Revision 3.1*
- *Serial ATA Specification*

This chapter does not cover the SATA-IO DC Coupled scheme referred to as DC coupled Gen1i.

The content of this section is for information only. For detailed information, refer the original specifications listed in Section 1.3~~listed paragraph 1.3~~.

6.8.1. AC Coupling Cap Values Per Respective Specification Definitions

The PCIe and USB3.1 specifications calls out for the AC Coupling Cap values as a function of interface signal transmission rate (~~ie~~e.g~~.e~~., Gen Speed).

PCIe and USB3.1 call out for AC Coupling Cap values given in Table 75 and Table 76 respectively. Table 77 lists the SATA-IO specification call outs for AC Coupling Cap values. Note that the SATA-IO specification calls out for AC Coupling Caps for both RX and TX.

Table 75. PCIe AC Coupling Cap Values

Designation	Description	Gen1	Gen2	Gen3	Units
C_{TX}	AC Coupling Capacitor	75 (Min) 265 (Max)	75 (Min) 265 (Max)	176 (Min) 265 (Max)	nF

Table 76. USB3.1 AC Coupling Cap Values

Designation	Description	Gen1	Units
C_{TX}	AC Coupling Capacitor	75 (Min) 200 (Max)	nF

Table 77. SATA-IO AC Coupling Cap Values

Designation	Description	Gen1/2/3	Units
C_{TX}	AC Coupling Capacitor	12 (Max)	nF
C_{RX}	AC Coupling Capacitor	12 (Max)	nF

6.8.2. AC Coupling Cap Location Examples

The PCIe, USB3.1, and SATA-IO specification all call out for the need to incorporate AC Coupling Caps on the highspeed differential signals.

6.8.2.1. PCIe and USB3.1 AC Coupling Cap Location Examples

The PCIe and USB3.1 specification calls out for the AC Coupling Caps to be located adjacent to the Transmitter. However, the specifications distinguish between two basic cases:

- Pluggable ~~Module~~Add-in Card
- All On the Same Board

For the Pluggable Add-in Card~~Module~~, the specification clearly indicates *Capacitors must be placed on the Transmitter side of an interface that permits adaptors to be plugged and unplugged*. Visually, this is shown in Figure 145.
One should assume that this convention is applicable to all the connectorized/pluggable version of the M.2 form factors.

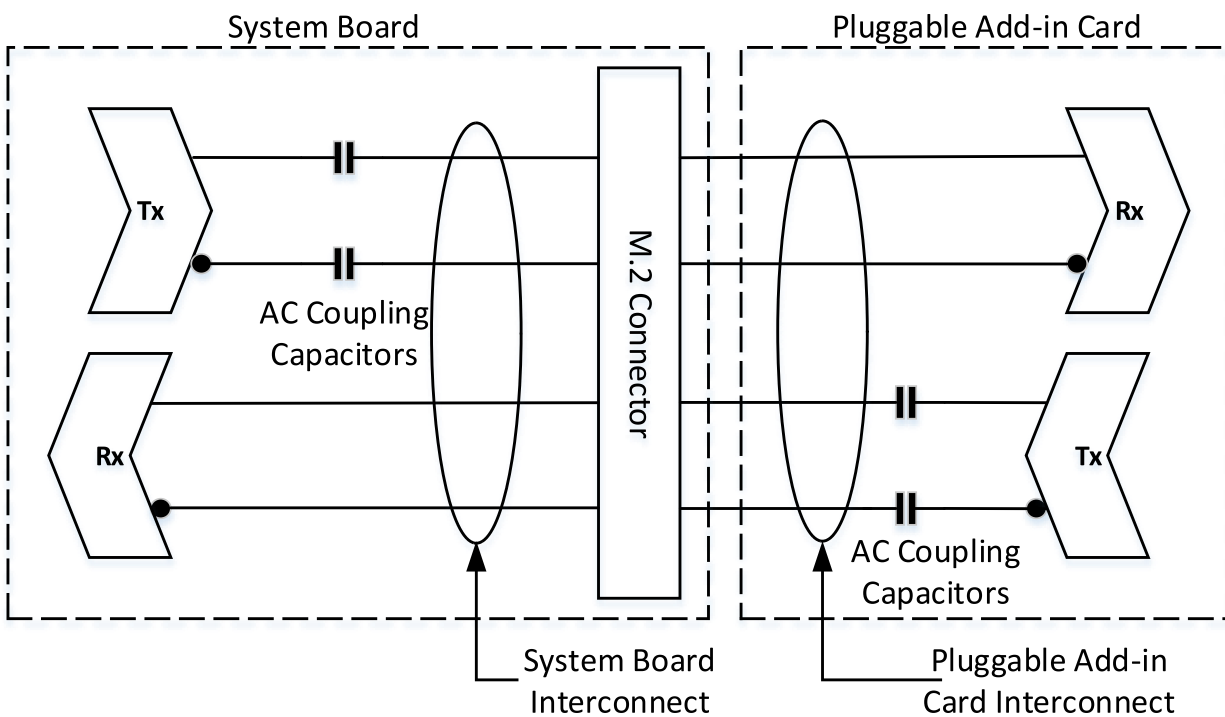


Figure 145. AC Coupling Cap Location – PCIe and USB3.1 Pluggable ~~Module~~ Add-in Card Example

Because of the integrated component nature of the M.2 family of LGA soldered down M~~m~~odules, this pluggable ~~module~~ Add-in Card convention should also be applied to the M.2 Type 1216, Type 2226, and Type 3026 soldered down M~~m~~odules even though there is not an actual connector. In this case the LGA footprint on the system board shows the connection point. The AC Coupling caps are adjacent to the transmitters with a set on the system board near the transmitter and a set on the ~~module~~ Add-in Card near its transmitter, as shown in Figure 146.

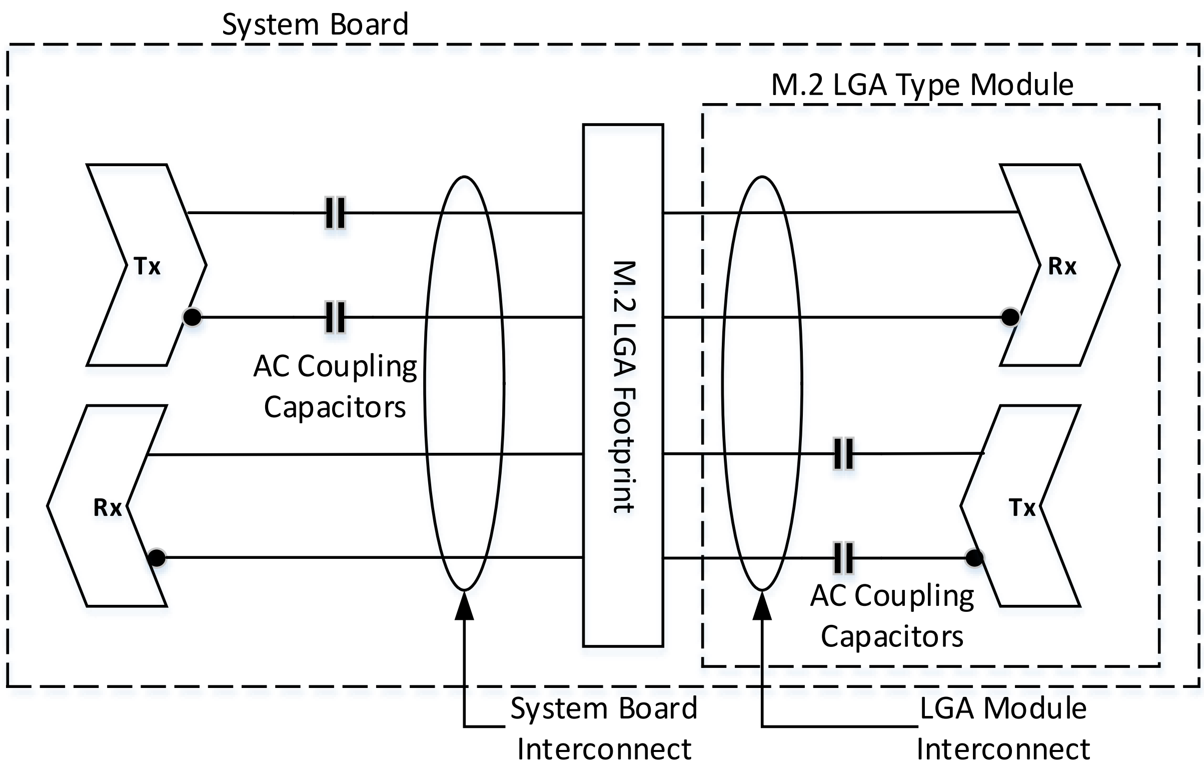


Figure 146. AC Coupling Cap Location – Soldered Down LGA Module on System Board Example

For the All-On-Same-Board case, the PCIe and USB3.1 specs indicate that when both the transmitters and both receivers are all on the same board, the AC Coupling Caps ~~can~~ are permitted to be placed anywhere along the signal lines. This definition is applicable to the M.2 family of SSD BGA Packaged devices. In this case, the AC Coupling Caps need to be somewhere along the signals paths as shown in Figure 147.

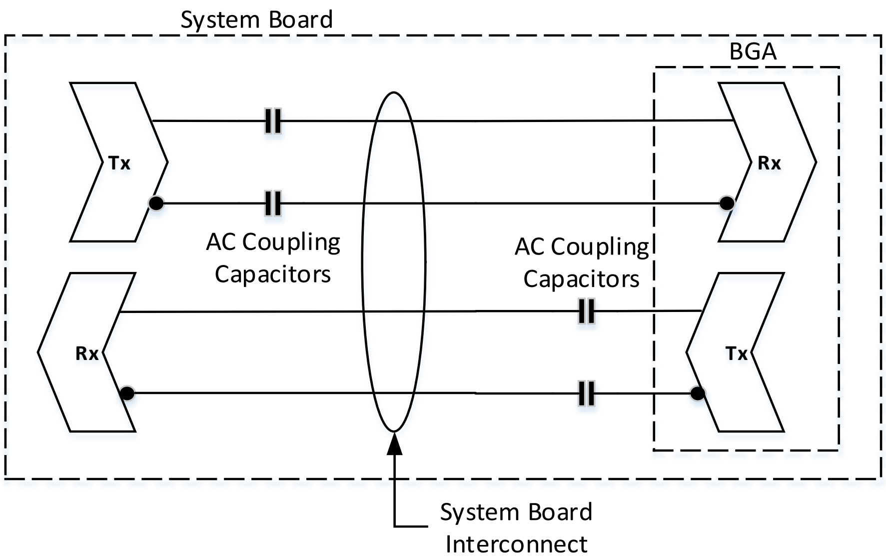


Figure 147. AC Coupling Cap Location – All-On-Same-Board Example

When an M.2 SSD BGA package device is mounted on an M.2 pluggable form factor, then the Pluggable Case should be applied. In this case, the AC Coupling Cap pair will be near the system board transmitter and the other pair will be on the M.2 ~~Module~~ Add-in Card on which the M.2 SSD BGA package is mounted, as shown in Figure 148. Since these are High Speed Differential Pair signals, it is highly recommended that Differential Line layout design rules be applied to the traces and the AC Coupling Caps for optimal signal integrity.

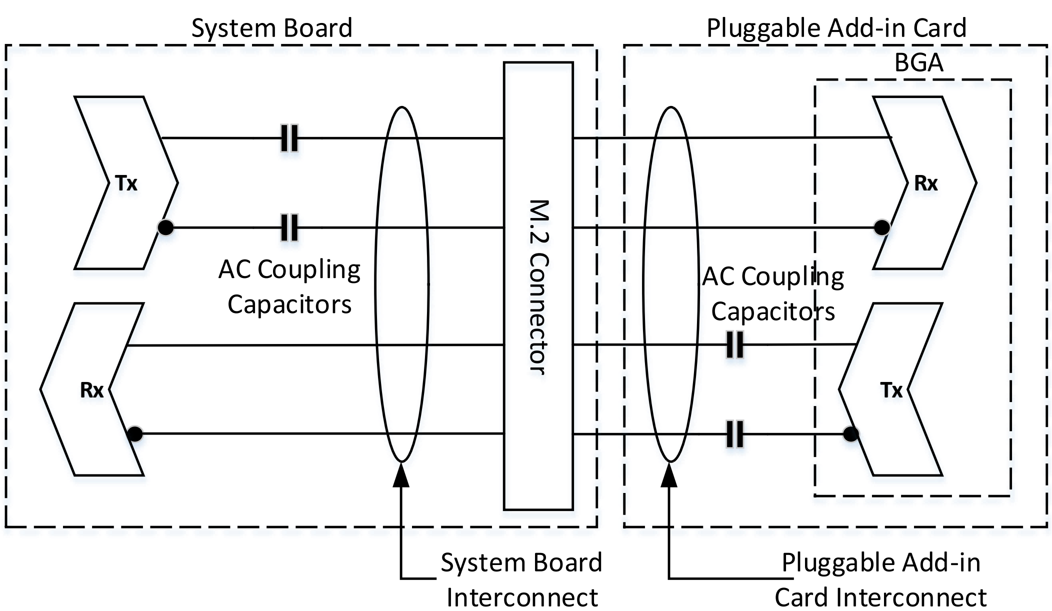


Figure 148. AC Coupling Cap Location - SSD BGA on Pluggable M.2 Form Factor Example

6.8.2.2. SATA-IO AC Coupling Cap Location Examples

It should be noted that the SATA-IO specification defines the location of the AC Coupling Caps differently compared with the PCIe and USB3.1 specifications. The SATA-IO calls for all the AC Coupling Caps to be placed on the ~~Module~~ Add-in Card. ~~No AC Coupling Caps on the System Board.~~ When applying this to the M.2 connection scheme, as shown in Figure 149.

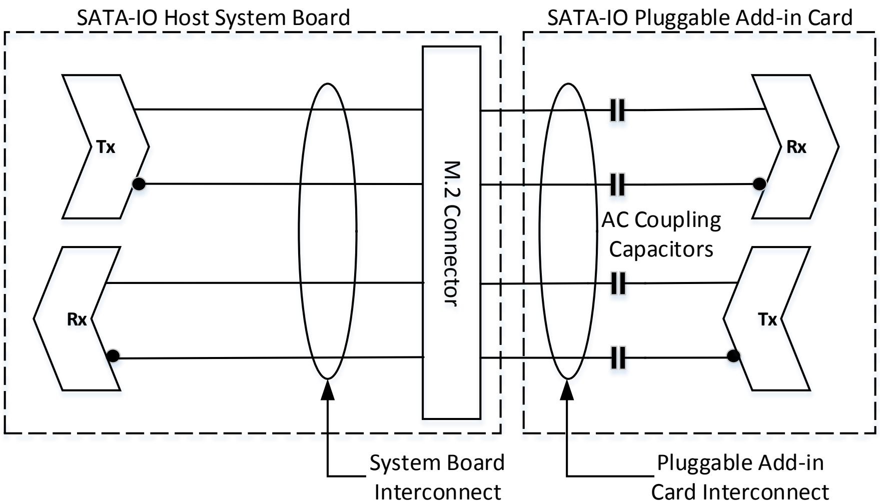


Figure 149. SATA-IO AC Coupling Cap Location – SATA Pluggable ~~Module~~ Add-in Card Example

Based on this convention, when an SSD BGA package is mounted on an M.2 ~~module~~ Add-in Card form factor, the AC Coupling Caps are located on the pluggable Add-in Card ~~module~~ but off the SSD BGA Package (see Figure 150).

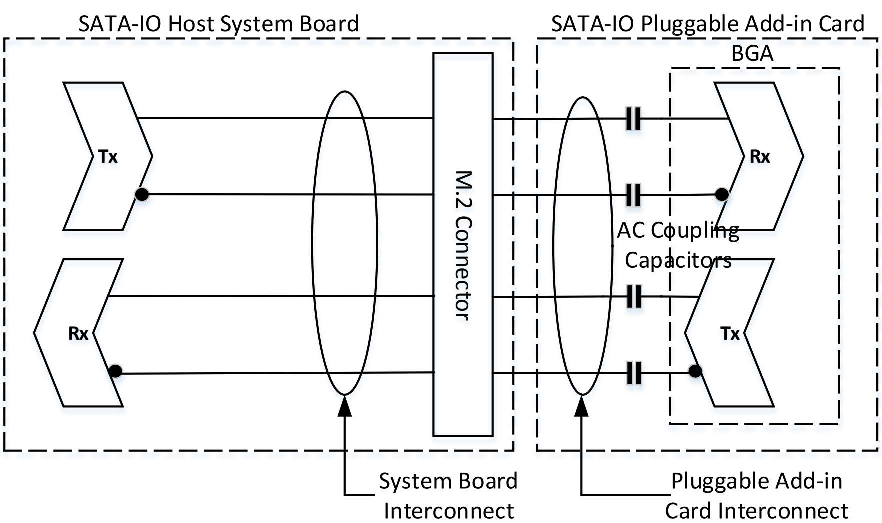


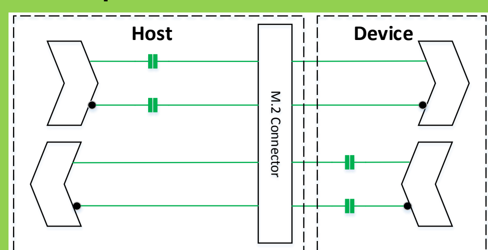
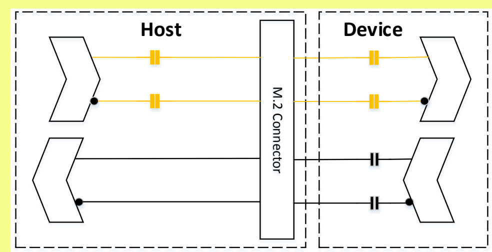
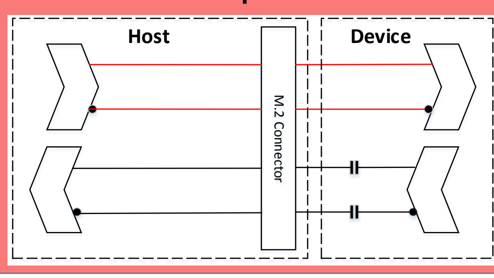
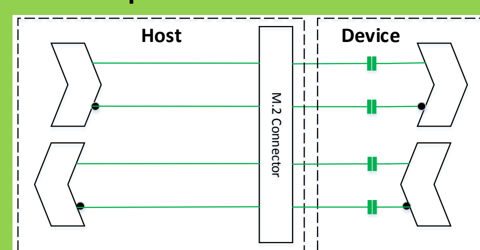
Figure 150. SATA-IO AC Coupling Cap Location - SSD BGA On Pluggable ~~Module~~ Add-in Card Example

6.8.3. AC Coupling Cap Scheme Compatibility Matrix

It is recommended that Host and Device AC Coupling Cap schemes match each other per the appropriate specification. SATA-IO and PCIe AC Coupling schemes differ from each other. System Board maybe designed to support PCIe and SATA-IO pluggable ~~modules~~Add-in Cards.

The matrix given in Table 78 shows the potential compatibilities and incompatibilities for all combinations.

Table 78. AC Coupling Cap Scheme Compatibility Matrix

	Device Designed According to PCIe/USB3.1	**Device Designed According to SATA-IO**
Host Designed According to PCIe/USB3.1	**Optimized for PCIe/USB3.1** 	**Compatible with PCIe/USB3.1 Gen1/SATA-IO [1]** 
Host Designed According to SATA-IO	**Incompatible [2]** 	**Optimized for SATA-IO** 

[1] Electrically, this case has two capacitors in series yielding a total capacitance which is still within SATA-IO specifications. However, the side-effects of serial capacitors may affect optimal signal integrity.

[2] DC coupling makes this incompatible for the both SATA-IO and PCIe/USB3.1.

6.9. Eye Limits for SSIC at the M.2 Connector

Transmitter Eye Height and Eye Width limits at the M.2 connector for the SSIC Host and the SSIC Device transmitter are defined in Table 79. This helps to test the interoperability between SSIC host and SSIC device at the M.2 connector. The eye diagrams are evaluated after the behavioral CDR defined in the *MPHY Specification* is applied. The eye limits given below are recommendations only.

Table 79. SSIC Transmitter Eye Limits at the Connector

	Eye Height at M.2 Socket	Eye Width at M.2 Socket	Notes
SSIC Device Transmitter	140 mV	0.6 UI_{HS}	1 to- 6
SSIC Host Transmitter	95 mV	0.55 UI_{HS}	1 to- 6

Notes:

1. Assumes the signal has been captured using a break-out fixture that is approximately 1-inch long (approximately -0.33 dB loss at ~~@~~1.455 GHz).
2. The recommended sample size for this measurement is at least 10^6 UI.
3. Eye measurements require that CRPAT (refer to *MIPI Alliance Specification for M-PHY*) is being transmitted during the test.
4. The measurements are applicable to Terminated HS mode of MPHY.
5. The Eye Width limits are applicable at Target BER of 10^{-10}.
6. The eye limits are applicable to the MPHY HS gears G1, G2, and G3.

A

Appendix A. Acknowledgments

Howard Andrews	Foxconn	Becky Loop	Intel Corporation
Doug Bennett	Intel Corporation	Fuqiang Ma	Huawei
Catherina Biber	Intel Corporation	Alan MacDougall	ACON
Hicham Bouzekri	ST-Ericsson	Jim McGrath	TE
John Carroll	Intel Corporation	Mike McKee	Foxconn
Josue Castillo	Luxshare-ICT	Glenn Moore	Foxconn
Conrad Choy	ACON	Robert Muir	Intel Corporation
Marty Czekalski	Seagate	Kazumi Nakazuru	Kyocera Connector
Robert Dmitroca	Intel Corporation	Manisha Nilange	Intel Corporation
Ricardo Espinoza-Iberra	Intel Corporation	Stefan Nilsson	Ericsson
Martin Furuhjelm	Seagate	Marc Noblitt	Samsung ~~&~~and Micron
Keqiang Gao	Huawei	James Panian	Qualcomm Technologies Inc
Will Harris	AMD	Rich Perry	Intel Corporation
Yongquan He	Huawei	Ed Poh	Molex Incorporated
Patrick Hery	Toshiba	Florence Pon	Intel Corporation
Larry Hsu	Bellwether	Jim Salembier	Lenovo
Jovica Jovanovski	Broadcom Corporation	Mark Saubert	JAE
Ramdas Kachare	Seagate	Brad Saunders	Intel Corporation
Kazushi Kamata	JAE	Chris Schmolze	Bellwether
Bilal Khalaf	Intel Corporation	David Shi	Huawei
Sammy Koyama	Kyocera Connector	Toshio Shimoyama	JAE
Dave Landsman	SanDisk	Takao Shirai	Toshiba
Jeff LeGassick	Intel Corporation	Nestor Sison	Sierra Wireless
Vince Smith	Sierra Wireless	David Wissel	Hewlett-Packard Company
Frank Sodek	AMD	Lei Xiang	Huawei
Ra’anan Sover	Intel Corporation	Su Yan	Intel Corporation

Chuck Stancil	Hewlett-Packard Company	Gregory Young	I-PEX
Cedrec Sumimoto	JAE	Pat Young	Luxshare-ICT
Tetsuya Tagawa	I-PEX	Andrew Zhang	Intel Corporation
Johan Uggmark	Ericsson	Long Zhao	Huawei
Scott Wallace	Sierra Wireless		

In Memoriam

This specification is dedicated to the memory of our friend and colleague, Marc Noblitt. Marc was a key contributor to the development of this specification right up until his passing in October 2013. Throughout his career Marc made many significant contributions to multiple computer industry standards and will be missed.